Present nanopatterning alternative and associated application opportunities

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Besides the development of EUV lithography addressing the high volume manufacturing segment for the production of future CMOS nodes, alternative nano-patterning techniques are under development and may offer credible and low cost patterning solutions for industry depending of the final application targets. This paper will review the status of three of the most promising techniques. In single exposure mode or in combination with other lithography solutions, they offer new attractive industrial options for the future of lithography. This work will also present how LETI supports and pushes their industrial insertions and promotes their fields of applications through collaborative industrial and institutional projects such as the IMAGINE and IDeAL programs respectively focused on multibeam and DSA techniques.

- Mask less lithography : after several year of prototyping demonstration, massively parallel electron writing enters in a new era with the availability of the first pre-production platforms for both wafer and mask writing[1]. MAPPER Lithography BV MATRIX platform is under assessment inside LETI 300 mm pilot line (Figure 1). A status of the capability of this technology with the latest results will be detailed in this paper.
- Directed self-assembly lithography : This complementary patterning option based on the self-assembly properties of block copolymer[2] has attracted a lot of attention those last years as it offers the possibility to achieve very high resolution at low cost taking advantage of the already installed patterning platform base in production. Industry is investigating how to introduce this technology to support advanced patterning capabilities. A review of the state of the art and its associated application will be presented.
- Imprint lithography : this patterning option [3], offers sub-10-nm spatial resolution, 3D shape manufacturing (Figure 3), that is of great interest for the cost-efficient manufacturing of hard disk drives, photonic devices, high-efficiency large-area photovoltaic, and integrated circuits. Latest wafer scale imprint developments in LETI will be reviewed in this paper.

References

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(3) S. Landis, NanoImprint Lithography, Nano Lithography, Wiley-ISTE, ISBN: 978-1-84821-211-4, page 87-168, January 2011.

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The research leading to these results has been performed in the frame of the industrial collaborative consortiums IMAGINE and IDeAL respectively focused on the development of MAPPER multibeam lithography and Directed Self-assembly technique by block copolymers.

Figure 1 : Outlook on the 1st Maskless MAPPER-SOKUDO lithography cluster LETI clean room environment

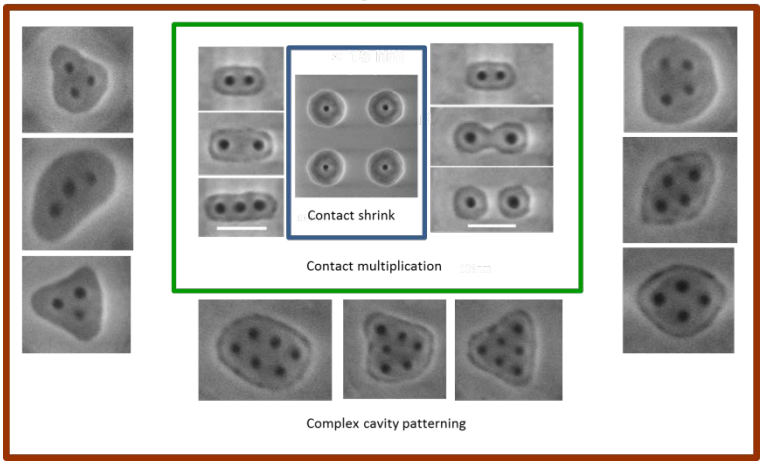

Figure 2 : Example of DSA patterning possibilities with grapho-epitaxy process flow

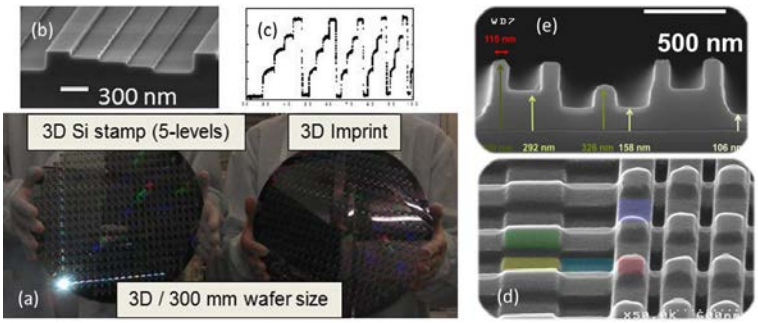

Figure 3: Outlook of imprint patterning realization at LETI site

(a) Photograph of the (left) 300 mm 3D Si stamp (with 5 levels) and (right) the corresponding printed 300 mm 3D resist coated over Si wafer.
(b) SEM picture of a Fresnel lens type pattern onto the Si stamp.
(c) Height measurement in a Fresnel lens type pattern printed into the resist.
(d) SEM picture of a multilevel cross bar pattern (each colour represent a resist thickness).
(e) SEM cross section view of printed resist with 5 different resist thicknesses ranging from 106 nm up to 500 nm. The critical dimension is 115 nm.