Readying Directed Self-Assembly for Patterning in Semi-Conductor Manufacturing

Roel Gronheid[a], Boon Teik Chan[a], Paulina Rincon Delgadillo[a,b,c], Arjun Singh[a,b], Joost Bekaert[a], Safak Sayan[d], Lieve Van Look[a], Yi Cao[e], YoungJun Her[e], Ainhoa Romo Negreira[f], Doni Parnell[f], Kathleen Nafus[f], Paul F. Nealey[c]

[a]imec, Kapeldreef 75, B-3001 Leuven, Belgium
[b]Katholieke Universiteit Leuven, Department of Electrical Engineering (ESAT), Kasteelpark Arenberg 10, B-3001 Leuven, Belgium
[c]Institute for Molecular Engineering, University of Chicago, 5747 South Ellis Avenue, Jones 222 Chicago, IL 60637, USA
[d]Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA 95054, USA
[e]AZ Electronic Materials, 70 Meister Avenue, Branchburg, NJ 08876, USA
[f]Tokyo Electron Europe, Kerkenbos 1015, Unit C, 6546 BB, Nijmegen, The Netherlands

Directed Self-Assembly (DSA) of Block Co-Polymers (BCP) has become an intense field of study as a potential patterning solution for future generation devices. DSA is a technique that is complementary to existing top-down projection lithography approaches based on 193nm immersion or EUV imaging. The most critical challenges that need to be understood and controlled for implementation of DSA into manufacturing include pattern placement accuracy, achieving low defectivity in DSA patterns and how to make chip designs DSA-friendly. The DSA program at imec includes efforts on these three major topics.

In this paper, an overview is given of activities at imec that are driving towards readying DSA technology for implementation into semi-conductor manufacturing. Flows for line/space and contact hole pattern formation based on chemo- as well as grapho-epitaxy are available and used for understanding process sensitivities and demonstration of integration approaches. The state-of-the-art of the various process flows is discussed in terms of defectivity, placement accuracy and how they may be implemented for device fabrication.