Nanofabrication of gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond

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As the gate pitch continues to scale down to accommodate the device density required for future technology nodes, the gate length of transistors is necessarily also reduced. This reduction, however, causes the degradation of transistor performance due to a loss of the electrostatic control of the channel. This effect can be mitigated by changing the gate geometry to control more sides of the channel. The gate-all-around (GAA) device–where all sides of the nanowire channel are surrounded by the gate–provides the ideal electrostatic control[1] and is one of the solutions the industry looks to for the 10 nm node and beyond.

Fabricating such a structure, however, poses significant challenges, as the devices are three-dimensional in nature. To start with, the nanowire channels need to be suspended to accommodate the gate-all-around geometry. In addition, making sub-10nm nanowire array with sufficient density to provide competitive drive current is difficult. We show that by using the developed hydrogen anneal process to address line edge and width roughness, ultra smooth, sub-10nm nanowire array can be reliably made down to the nanowire pitch of 30 nm. (Figure 1a) In addition, an active width equivalent to planar CMOS can be attained with a single level of nanowires[2].

Another unique fabrication challenge of the nanowire device is the gate stack patterning. Because of the suspended nature of the channel, patterning of the gate lines requires an additional step to remove the gate material from the underside of the suspended nanowires. This significantly adds to the complexity of gate patterning, particularly at tight gate pitch. We show an approach to address these issues and demonstrate gate patterning down to 60 nm pitch[2]. (Figure 1b)

Source-drain engineering of these devices presents additional challenges as the channel is three-dimensional. We show a novel cut-then-regrow source / drain approach to address this problem and obtain a more abrupt junction. With the developed *in situ* doped epitaxy source / drain growth, dopants can be vertically placed right at the edge of the spacer. This not only minimizes the diffusion distance but also yields a uniform gate length throughout the height of the device. (Figure 2a)

With the developed nanofabrication scheme, a high-density integration for both the nanowire pitch and the gate pitch was achieved[2]. (Figure 2)

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[1] S. Bangsaruntip *et al*., *IEDM Tech. Dig*., 2009 p. 297
[2] S. Bangsaruntip *et al*., *IEDM Tech. Dig*., 2013, 20.2.1.

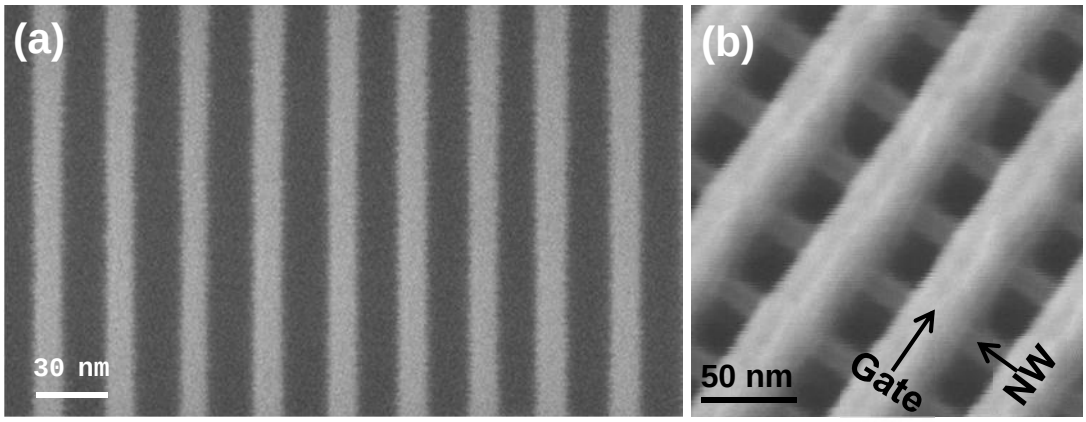

Figure 1: Scaled gate-all-around nanowire device: (a) An SEM image of a suspended silicon nanowire array at an aggressive pitch of 30 nm. Nanowires are well-smoothen using the developed hydrogen annealing process. The final LER achieved was 0.8 nm, at the level of our instrument limit. (b) A tilted top-down SEM view of multiple gate lines, at 60 nm pitch, patterned over suspended nanowires.[2]

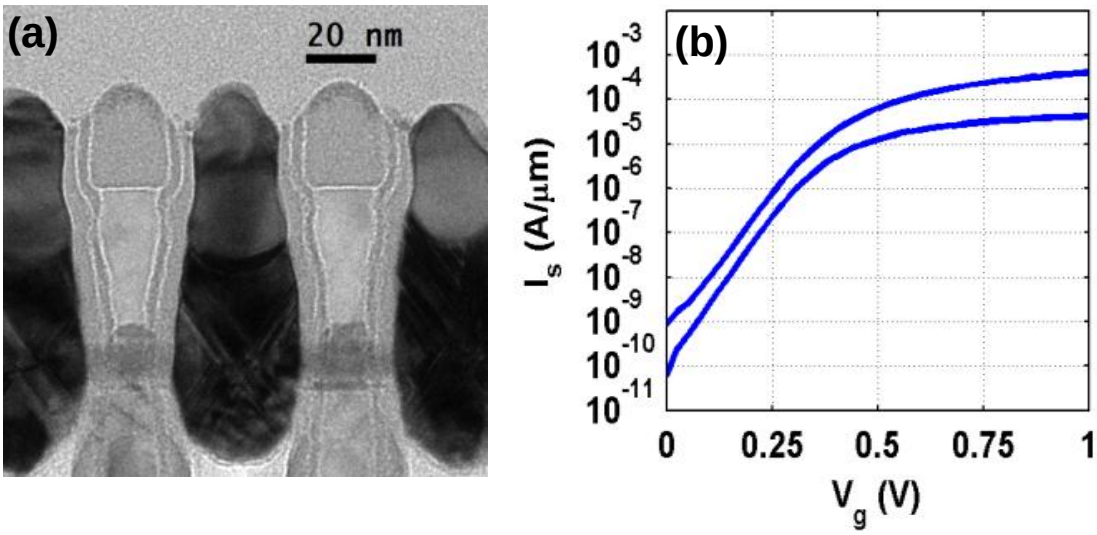

Figure 2: Fully fabricated gate-all-around silicon nanowire MOSFET: (a) Across-sectional TEM image of a fabricated device at gate pitch of 60nm, showing the *in situ* doped, raised epitaxy source / drain. (b) Transfer characteristic of an NFET with a 60 nm contacted gate pitch. The effective nanowire diameter was 8.1 nm and the physical gate length was ~15 nm.[2]