Varying gate layout nanowire single-electron defined by electron beam lithography

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Successful ‘beyond CMOS’ technology is likely to require new approaches to semiconductor electronic devices, in combination with lithographic and fabrication technology at the sub-5 nm scale[1]. In large-scale integrated (LSI) circuit applications, as planar MOSFET scaling limits are reached, in the near-term a transition may occur from non-planar fin-FET devices to Si nanowire FETs. Here, the channel cross-section can be scaled in both dimensions to ~10 nm, gates fully surround the channel, and the devices remain mainly ‘classical’ in nature. However, a far greater technological challenge is a subsequent transition to quantum-effect devices with scaling in all three dimensions to < 5 nm, e.g. single-electron and quantum-dot (QD) based devices. These devices, unlike ‘classical’ devices, inherently tend to improve in performance with reduction in size.

In this work, we report the fabrication and measurement of single-electron transistors (SETs)[2] defined in silicon-on-insulator (SOI) material. The devices are based on heavily doped, oxidised Si nanowires (NWs), with dual in-plane side gates and are fabricated by electron beam lithography (EBL) (Fig. 1). The gate voltage can be used to turn off the NW current. Near threshold, the variation in the NW potential due to disorder and pattern-dependant oxidation (PADOX), creates charging ‘islands’ isolated by tunnel barriers and forms the SET. This implies that the island/tunnel barrier configuration can be controlled by the shape of the side-gates. The SETs were measured from 8 - 300 K and single-electron operation was established from 8 K to ~220 K. ‘Coulomb staircase’ drain-source current (I_{ds}) vs. drain-source voltage (V_{ds}) characteristics are observed at 8 K (Fig. 2 and 3), and the Coulomb gap could be modulated periodically by gate voltage V_{gs}. The Coulomb staircase persisted to ~220 K. Single-electron Monte Carlo simulations have been used to explain the details of these characteristics. SET operation may be explained by formation of a multiple-tunnel junction along the Si NW.

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[1] Durrani Z, Jones M, Kaestner M,Hofer M, Guliyev E, Ahmad A, Ivanov T, Zoellner J-P, Rangelow I: Proc SPIE v8680 17: pp 1-12 (April 2013)
[2] Likarev K K : Proc IEEE, Vol. 87, pp 606-632, (1999)

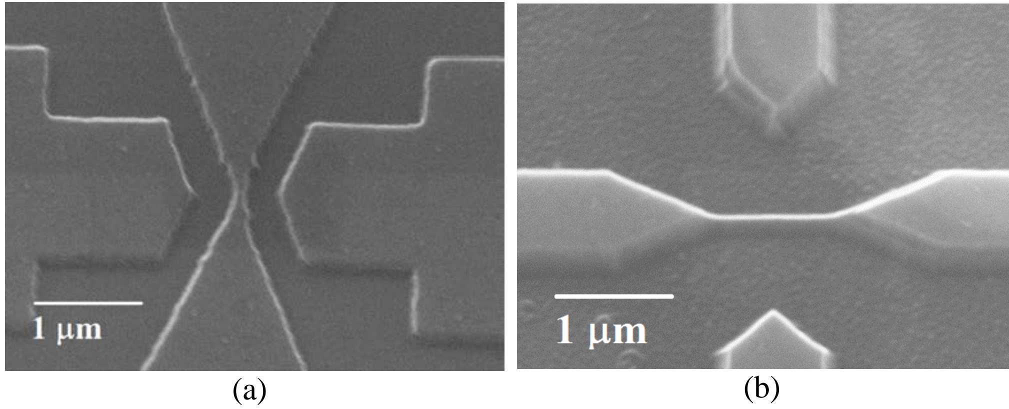

Figure 1. (a) SEM image of a Si NW SET with dual, in-plane gates parallel to the NW. (b) SEM image of a NW SET with gate lengths reduced to form a ~20 nm wide tip

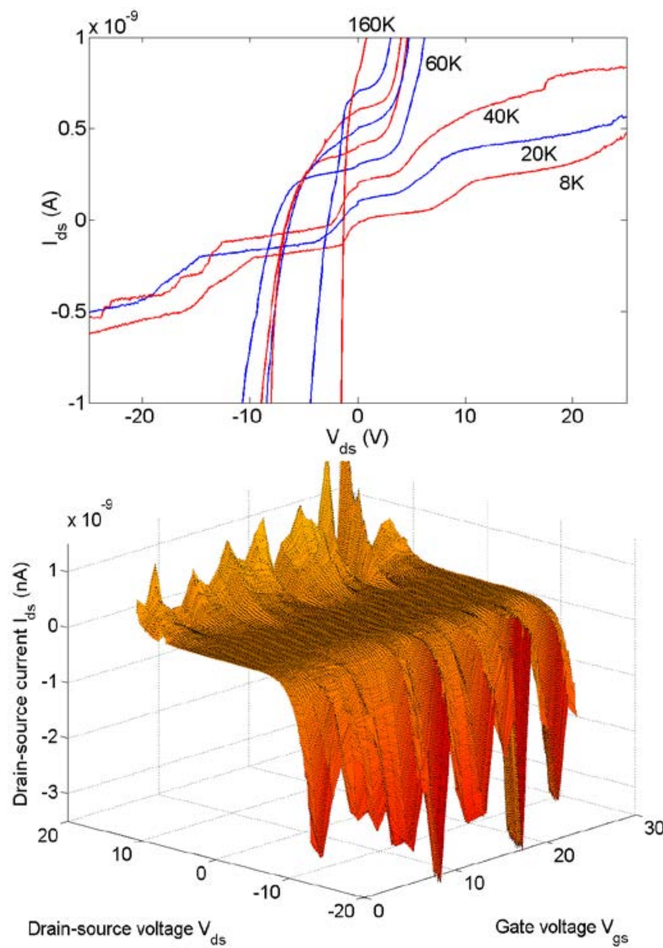

Figure 2. Coulomb staircase I_{ds}-V_{ds} characteristics in a Si NW SET, from 8 – 160 K. Curves offset 0.1 nA per temperature step for clarity.

Figure 3. Coulomb staircase at 8 K, modulated by gate voltage V_{gs}.