Progress Towards NEMS Devices based on STM-fabricated Hydrogen Depassivation Patterns

Josh Ballard,¹ Jason Gorman,² Neil Sarkar,³ Don Dick,⁴ Joseph Fu,² Rahul Saini,¹ James Owen,¹ Yves Chabal,⁴ John Randall,¹ Jim Von Ehr¹ ¹Zyvex Labs, 1321 N. Plano Road, Richardson, TX ²National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD20899 ³ICSPI, 248 Corrie Cr., Waterloo, ON Canada N2L 6E1 ⁴University of Texas at Dallas, 800 W. Campbell Rd., Richardson, TX 75080

The reduction in size of Nano-Electro-Mechanical Systems (NEMS) holds the promise of increasing the sensitivity of mass sensors, pushing the limits of high-frequency resonators, or enabling previously unavailable mechanical quantum systems. However, with the size comes a requirement for even greater precision in fabrication—the uncertainty in feature geometry must at least scale with the size of the feature else the unique device characteristics may become unpredictable. To address this limitation, a Scanning Tunneling Microscope (STM) is used to pattern a surface with near atomic precision, with those patterns transferred into silicon, after which the NEMS structures are to be released and characterized.

STM-based Hydrogen Depassivation Lithography (HDL) has previously been shown to be able to produce depassivation patterns with size scales ranging from a single atom to several microns in size[1]. These HDL patterns have also been shown to have chemical selectivity with many species showing patterned deposition[2]. Here, TiO₂ is selectively deposited using Atomic Layer Deposition (ALD) with size and shape control down to the nanometer scale[3]. Furthermore, TiO2 deposited on silicon has been shown to act as a selective etch mask against Reactive Ion Etching (RIE), allowing fabrication of 3-D structures with CD down to a few nanometers while maintaining registration with the atomic lattice due to the intrinsic metrological capabilities of the initial HDL patterning step [in preparation, see fig. (1a)].

Release of these atomically precise 3-D structures will be discussed, with technologies including Nano-SCREAM[4] to release Si on Si structures as well as standard HF release of structures from SOI wafers. Geometric limitations of the processing conditions will also be discussed, including the maximum NEMS feature height, as well as maximum and minimum lateral feature dimensions using patterns similar to fig. (1b). Within these constraints, progress towards fabrication of various structures will be presented. Comparisons of fabricated structures with atomic scale FEA predictions will be presented [see fig. (2)], along with a perspective on the range of devices that are enabled with this fabrication technology with traceability to the Si(100) atomic lattice.

- [1] J. B. Ballard, T. W. Sisson, J. H. G. Owen, W. R. Owen, E. Fuchs, J. Alexander, J. N. Randall, and J. R. Von Ehr, "Multimode hydrogen depassivation lithography: A method for optimizing atomically precise write times," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 31, no. 6, p. 06FC01, 2013.
- [2] M. C. Hersam, N. P. Guisinger, and J. W. Lyding, "Silicon-based molecular nanotechnology," *Nanotechnology*, vol. 11, no. 2, pp. 70–76, Jun. 2000.
- [3] S. McDonnell, R. C. Longo, O. Seitz, J. B. Ballard, G. Mordi, D. Dick, J. H. G. Owen, J. N. Randall, J. Kim, Y. J. Chabal, K. Cho, and R. M. Wallace, "Controlling the Atomic Layer Deposition of Titanium Dioxide on Silicon: Dependence on Surface Termination," *J. Phys. Chem. C*, vol. 117, no. 39, pp. 20250–20259, Oct. 2013.
- [4] N. C. MacDonald, "SCREAM MicroElectroMechanical Systems," *Microelectron. Eng.*, vol. 32, no. 1–4, pp. 49–73, Sep. 1996.



Figure 1: STM initiated nanopatterns. a.: Portion of an 800 nm x 800 nm serpentine pattern fabricated by STM-HDL, ALD, and RIE. The constituent lines are 12 nm wide and 17 nm tall. b.: Hard mask pattern of a variety of release test 76 nm pads and connector link widths from 7 nm to 38 nm.



Figure 2: Simulation of third mode of I^2 bar NEMS structure. The blue pads are immobile. The simulated device is 350 nm along the pad axis, 380 nm wide, and 200 nm tall.