Thermal Probe Nanolithography: What You See is What You Get

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Thermal Scanning Probe Lithography (tSPL) is an AFM based patterning technique, which uses heated tips to locally evaporate organic resists such as molecular glasses [1] or thermally sensitive polymers [2]. Patterning quality is excellent up to a resolution of sub 15 nm [1], at linear speeds of up to 20 mm/s and pixel rates of up to 500 kHz.[3] The patterning depth is proportional to the applied force which allows for the creation of 3-D profiles in a single patterning run.[2]

For reliable patterning at high speed and high resolution an efficient control system is essential. Here I will discuss how we implemented a closed-loop lithography control scheme. We obtain the control signals by reading the topography in the retrace motion of the scan, while writing is performed during the trace motion. We use the acquired data to optimize the position stability in vertical direction, the amplitude and offset of the applied writing force and the applied force during reading. Here we demonstrate that depth levels are reproduced with an accuracy of about 1 nm (Fig. 1).

These novel patterning capabilities are equally important for a high quality transfer of two-dimensional patterns into the underlying substrate. We utilize an only 3-4 nm thick SiOx hardmask to amplify the 8±0.5 nm deep patterns created by tSPL into a 50 nm thick transfer polymer. Here we demonstrate the fabrication of 27 nm wide lines and trenches 60 nm deep into the Silicon substrate [4] (Fig. 2).

The stable registry originating from the combined read and write operation allows one to perform marker-less pattern overlay at nanometer accuracy (Fig. 3). For demonstration we structured a Silicon wafer by optical lithography to obtain 1 micron wide and 5 to 110 nm tall features. After deposition of the pattern transfer stack the topography is reduced and blurred by the spin coating process. We show theoretically, that our correlation based marker-less registration scheme allows us to detect the position of the Silicon structures with an accuracy of about 1/200th of the feature size in Silicon.

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[2] A. W. Knoll et al., *Adv. Mater.* **22**, 3361 (2010).
[3] P. Paul et al., *Nanotechnology* **22**, 275306 (2011).
[4] L. L. Cheong et al., *Nano Lett.* (2013), DOI: 10.1021/nl4024066.

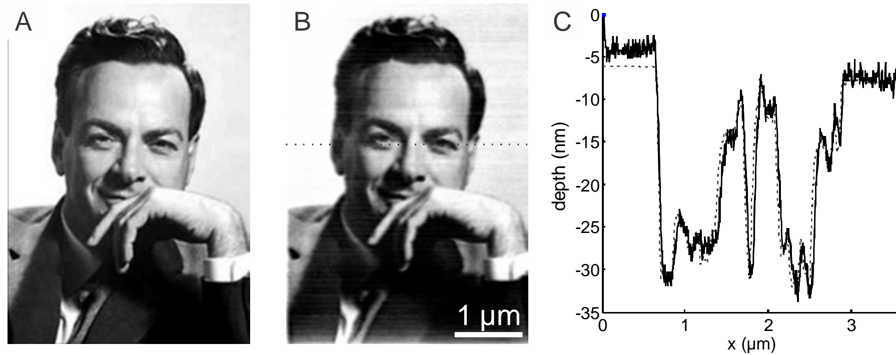

Figure 1. 3D reproduction of a grayscale photograph of Richard Feynman, source: Wikipedia. A) Programmed bitmap of size 400x560 pixels. The programmed target depth extends from -6 to -35 nm. B) Topographical image of the three dimensional reproduction. The gray scale ranges from -6 to -35 nm. C) Cross sectional profile along the dotted line plotted in panel B, both for the programmed pattern (dashed) and the recorded topography (full line).

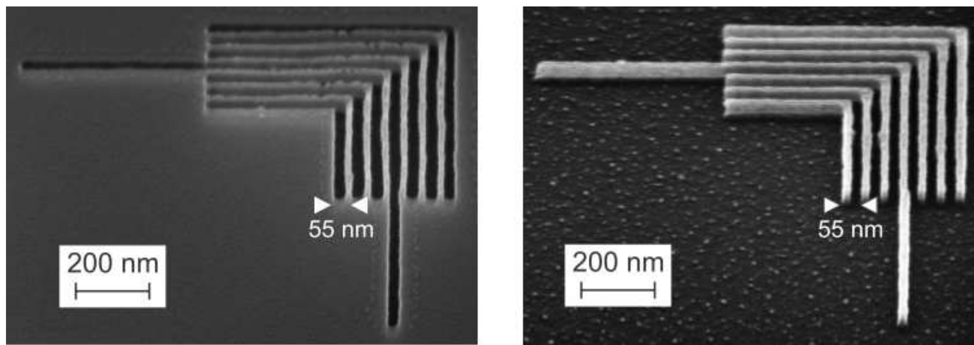

Figure 2. Nested L-lines created in Silicon at a pitch of 55 nm. Both the normal and the inverse pattern were created side by side without correction of the patterning parameters.

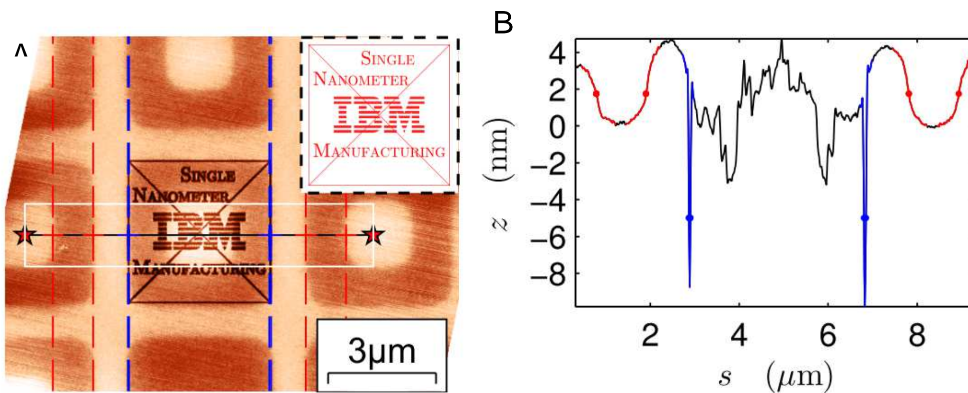

Figure 3. Marker-less overlay on buried Si structures. A) AFM topography image of the final overlay result. The optical pattern is visible as micron wide features in the image. The tSPL written pattern is shown in the inset. B) Average cross-section according to the white box in A. Edge detection using the red and blue dots yields an overlay error of 3.2 nm.