Reusable Silicon Templates for Fabricating Sub-10-nm Grooves In Metal Films

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Template stripping of gold or silver films off a silicon substrate has been applied to fabricate ultra-flat substrates for research in scanning-probe microscopy,¹ plasmonics,² and molecular junctions.³ Template stripping relies on the deposition the metal film on a substrate, and detaching it using adhesives onto another handle wafer. Recently, template stripping from patterned silicon substrates has attracted significant attention due to its ability to fabricate various plasmonic structures with ultra-smooth surfaces, which is critical to reduce damping losses.^{4,5} We demonstrate the extension of the template-stripping technique down to sub-10-nm feature dimensions.

Figure 1 presents scanning electron microscope (SEM) images of silicon templates with silicon lines patterned in a square and triangular grid. The linewidth was measured to be \sim 8 nm. Figure 2 shows gold films that have been patterned via the template-strip technique to create nanogrooves that support localized plasmon resonances. The tapered cross section of the template results in 12-nm-wide grooves on the surface that narrow to sub-10-nm dimensions in the trenches.

We will report the fabrication of these templates, the template stripping process, and the reusability of the templates. We will explore several potential applications of these gold substrates, e.g. V-groove plasmon waveguides and surface-enhanced Raman scattering substrates.

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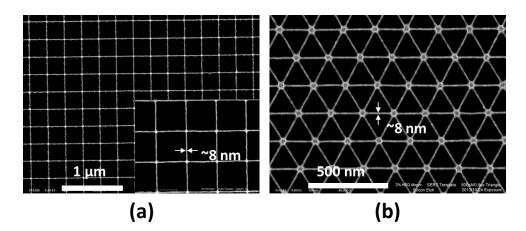


Figure 1: SEM images of the silicon template with a line width of 8 nm for template stripping: (a) Square-grid patterns with a pitch size of 290 nm; (b) Triangular-grid patterns with a side length of 200 nm.

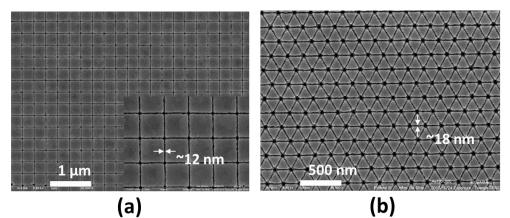


Figure 2: Template stripped gold substrates: (a)-(b) SEM images of the square and triangular arrays where the dark lines are grooves in a gold film.