The Litho Roadmap: Is it a straight path?

Michael Lercel, Mark Neisser, and Kevin Cummings SEMATECH Inc, Albany NY 12203

Lithography improvements have enabled a long-lived steady increase in device density for the semiconductor industry. Several innovations in lithography have occurred over the past few decades to enable this scaling trend. New technologies, such as EUV and direct-write e-beam, have been under development as the "next generation lithography" technologies. However, continuing challenges with these means they remain "next generation lithography" and not current high-volume manufacturing solutions. So is this the end of scaling and Moore's law if these technologies are not successful? Perhaps not – what exactly is scaling and the roadmap? The assumption has always been a full scaling of dimensions, tolerances, and defectivity all at the same time. Is that the right definition?

In this paper we will examine the current state of "next generation lithography" techniques from a technical, yield, and cost standpoint, and then explore trends in lithographic scaling for dimensions, tolerances, defectivity, and cost to see if the straight linear assumptions of the roadmap still hold true. This analysis will be applied to multiple patterning, EUV, ebeam direct write, nanoimprint, directed self-assembly, and other options.