An anisotropic low power, low DC bias, SF_6/C_4F_8 inductively coupled plasma etch process of molybdenum with critical dimension of 30 nm suitable for compound semiconductor devices

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Although the mainstream semiconductor industry will always be silicon-based, compound semiconductor devices have an important role to play in high frequency & ultra-low power applications. As a result, III-V on silicon substrates are being actively developed[1]. In parallel, there is a need to establish nanoscale III-V device processes using standard silicon manufacturing approaches such as anisotropic dry etch processes for metal gates, with very low power and DC bias to minimise mobility degradation. Although molybdenum has previously been utilised in gate fabrication of silicon MOSFET & FinFET[2], power levels of at least 100 W were used in the etch processes. Such high power levels when etching dielectrics and metals have previously been shown to severely degrade the mobility of III-V materials[3,4] & as a result, power levels of less than 20 W are a typical requirement for "damage-free" dry etching processes in compound semiconductors.

This paper presents an anisotropic SF_6/C_4F_8 inductively coupled plasma (ICP) process for etching molybdenum with critical dimension of 30 nm. The low platen power used in the etching system has previously yielded low damage etching[3,4], making the process reported here an attractive candidate for the realisation of short gate length III-V high electron mobility transistors using silicon like, “lift-off free” approaches.

A 100 nm molybdenum film was deposited by electron beam evaporation on a GaAs substrate, which was then spin coated with 150 nm HSQ resist. Lines with designed sizes in the range 15 nm-50 nm were then defined by 100 keV electron beam lithography using a Vistec VB6 UHR-UWF tool. Figure 1 shows a cross sectional electron micrograph of one of the HSQ lines after development. A Surface Technology System Ltd. ICP etching system was used for the SF_6/C_4F_8 etch process optimisation. SF_6 etches the molybdenum by generating volatile molybdenum fluorides, whilst C_4F_8 passivates the etched sidewalls thereby enabling high resolution, anisotropic etching at low power and DC bias. Gas ratio, coil and platen powers, and chamber pressure were the variables explored in the process optimisation. Figures 2 and 3 show the influence of platen power and chamber pressure on the vertical etch rate of molybdenum and also average bias voltage with the flow rates of SF_6/C_4F_8= 15 sccm/25 sccm. The low platen power levels and DC bias are the particularly noteworthy features. As shown in Figure 4, 30 nm critical dimension molybdenum features, to our knowledge the highest resolution patterns transferred by dry etching into molybdenum to date, can be realised with a platen power as low as 2W, a key requirement for low damage etching of metal gates in high performance compound semiconductor devices.

[1] L. Czornomaz et al, Proc. IEDM 2013, pp52-55, 2013
[2] D. Ha et al., IEEE Trans. Electron Dev., 51, 12, pp1989-1996, 2004
[3] X. Li et al., Microelectron. Eng., 85, 5-6, pp996-999, 2008
[4] X. Li et al., Microelectron. Eng., 83, 4-9, pp1152-1154, 2006

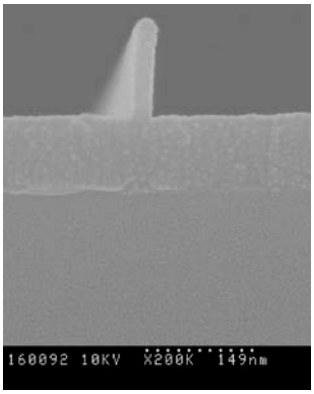

Figure 1. SEM image of cross-sectional profile of the HSQ line after development. Scale bar is 149nm.

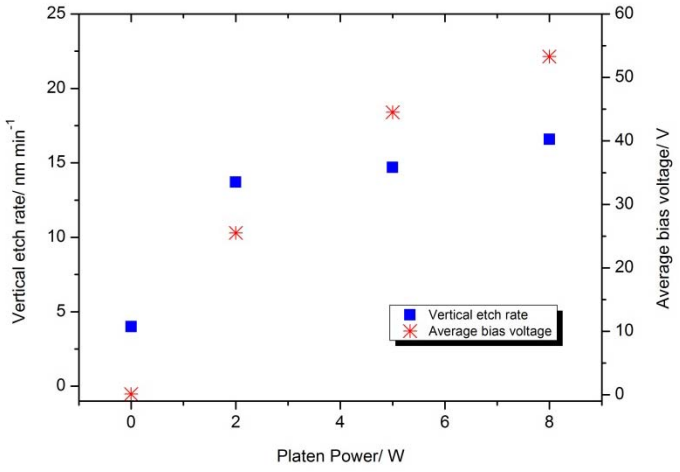

Figure 2. Vertical etch rate & Average bias voltage as a function of platen power, with chamber pressure of 5mTorr, SF_6/C_4F_8=15/25 sccm.

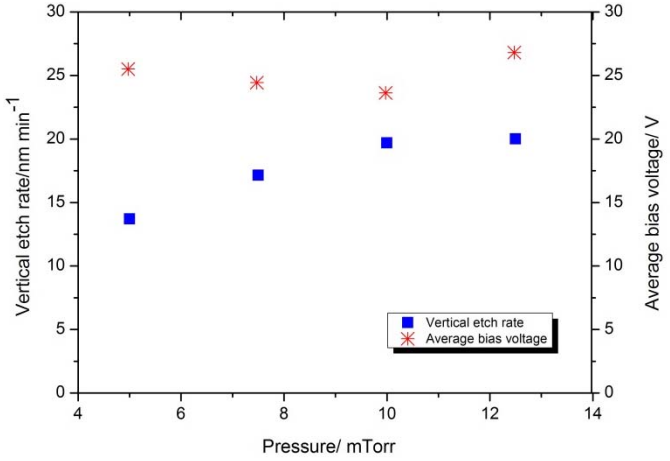

Figure 3. Vertical etch rate & Average bias voltage as a function of chamber pressure, with platen power of 2W, SF_6/C_4F_8=15/25 sccm.

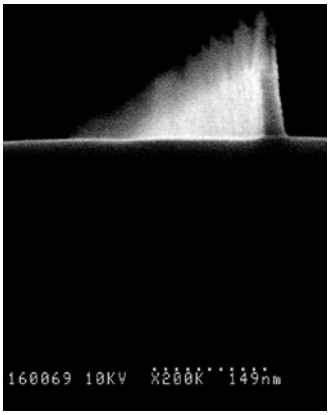

Figure 4. SEM image of 30 nm critical dimension molybdenum features, with platen power 2W, chamber pressure 5mTorr, SF_6/C_4F_8=15/25 sccm. Scale bar is 149nm.