# Focused Ion Beam milling for Si nanowire and Junctionless transistor prototype

L.P.B. Lima[1,2], M.V. Puydinger dos Santos[1], J. Godoy Filho[1], H. F. W. Dekkers[3], S. De Gendt[2,3], J. A. Diniz[1]
[1]School of Electrical Engineering, University of Campinas, 13083-970 Campinas, Brazil
[2]Chemistry Department, KULeuven, Leuven, Belgium
[3]Imec, Kapeldreef 75, 3000 Leuven, Belgium
*lucas@ccs.unicamp.br*

Recently, Focused Ion Beam (FIB) system has been used in transmission electron microscopy (TEM) and also for micro and nanofabrication, as application in circuit editing and prototype nanomachining.[1] One advantage of using FIB system is that it does not require lithography for milling (for example, Si milling) and has nanometric resolution. Also, some surface damage or ion incorporation on substrate surface can occur due to gallium ($Ga^+$) FIB milling which leads into changes on substrate optical and electrical properties.[2] However, this effect is desirable in some cases and FIB system can be also used for ion implantation.[3,4] In addition, FIB system can deposit metallic and dielectric layers, such as platinum (Pt) and silicon dioxide ($SiO_2$), respectively. In this context, nMOS Junctionless (JL) devices were fabricated on silicon-on-insulator (SOI) substrates using $Ga^+$ FIB for Si milling and depositions of $SiO_2$ (gate dielectric) and Pt layers (as gate, drain and source electrodes) of JL transistor. JL devices have gained much attention of microelectronics industry, because it is compatible with CMOS technology and can be useful for 3D devices.[3,5] Also, these devices present low leakage current, good subthreshold slope, and, at high temperature, present high mobility and little diffusion of impurities.[5] In this work, two methods to fabricate the JL devices were used. The first method is to use FIB system for milling the Si substrate and define SiNW. For the second method Reactive Ion Etching (RIE) and FIB system were used to define the MESA structure and SiNW, respectively, in order to minimize the $Ga^+$ ion incorporation on SiNW surface. The samples with only FIB system were called JLFIB (Figure 2a) and samples with RIE plasma etch and FIB system were called JLRFIB (Figure 2b). The SOI samples were doped with phosphorus, dose $10^{19}$ $cm^{-3}$ and energy of 30 KeV, using ion implantation system, and Rapid Thermal Annealing (RTA) was used to anneal the samples after ion implantation procedure. The SiNW were obtained using $Ga^+$ FIB milling, defining the gate, drain and source regions of JL transistors (Figure 1a). The SiNW widths were around 100 nm and 50 nm, while the length was about 4 µm. In addition, two different SiNW heights were used, around 50 nm and 15 nm, in order to achieve better control of JL channel. The 10-nm-thick $SiO_2$ (used as gate dielectric) and 200-nm-thick Pt (used as gate, drain and source electrodes) were deposited by FIB system. Energy Dispersive X-Ray Spectroscopy (EDS) measurements were carried out to confirm the surface composition of SiNW (Figure 1b), $SiO_2$ gate dielectric deposition (Figure 1c) and Pt electrodes deposition (Figure 2c). EDS measurements show Ga incorporation on SiNW surface due $Ga^+$ FIB milling process. Drain-source current ($I_d$) x drain-source voltage ($V_{ds}$) measurements of JLFIB (Figure 3a) and JLRFIB (Figure 3b) devices were carried out, and indicate that the devices are working like a gated resistor or JL device. The extracted values for sub threshold slope (SS), shown in Figure 3c, are lower than 100 mV/decade and were obtained for different bias from bulk polarization ($V_{bulk}$). Finally, our fabrication method using FIB process steps (Si milling, $SiO_2$ and Pt depositions) can be used to obtain nanowire based devices, such as JL transistors.

[1] K.A. Unocic, M.J. Mills, G.S. Daehn, J. of Micros., 240, 227 (2010).
[2] H.X. Qian, W. Zhou, J. Miao, L.E.N. Lim, X.R. Zeng, J. Micromech. Microeng., 18, 35003 (2008).
[3] M.V. Puydinger dos Santos, L.P.B. Lima, J.A. Diniz, J. Godoy Filho, J. Vac. Sci. Technol. B, 31, 06FA01 (2013).
[4] D. Cooper, R. Truche, A.C.T. Harrison, R.E.D. Borkowski, P.A. Midgley, J. of Micros., 233, 102 (2009).
[5] J.P. Colinge, I. Ferain, A. Kranti, C.W. Lee, N.D. Akhavan, P. Razavi, R. Yan, R. Yu, Sci. Adv. Mat., 3, 477 (2011).

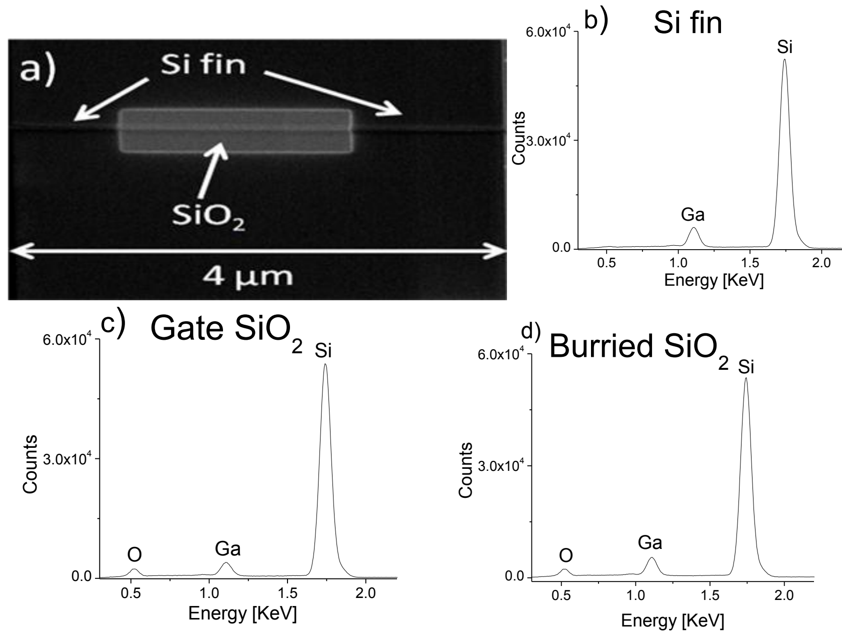


*Figure 1:* a) SiNW with gate $SiO_2$ deposited. EDS measurements of b) SiNW, c) gate $SiO_2$ deposited by FIB system and d) burried $SiO_2$ of SOI waffers.

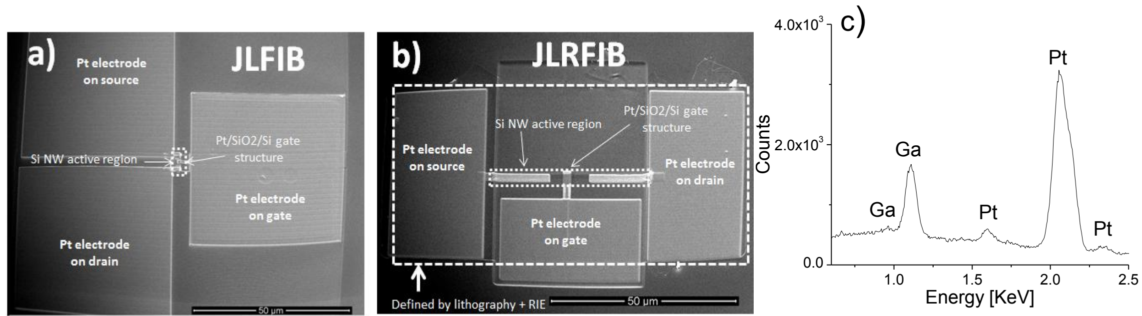


*Figure 2:* a) Final JLFIB device. b) Final JLRFIB device. c) EDS measurements of Pt electrode deposited by FIB system.

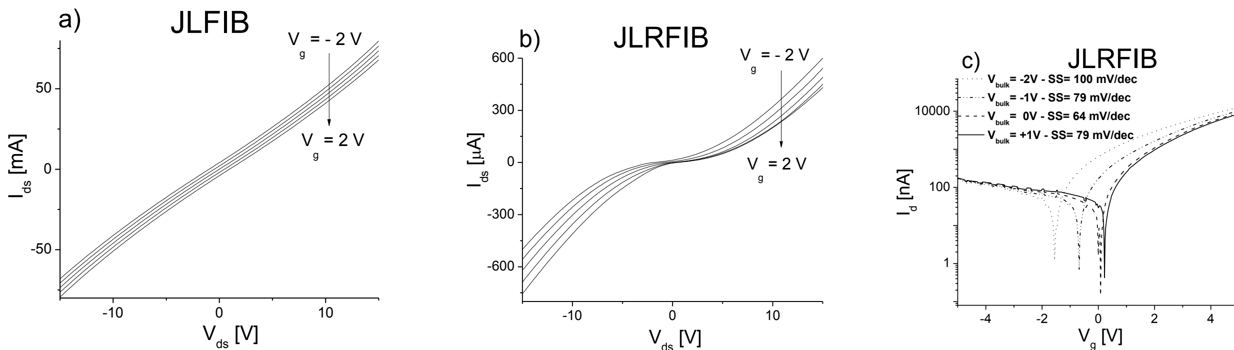


*Figure 3:* $I_d$ x $V_{ds}$ measurements of a) JLFIB; b) JLRFIB. c) $I_d$ x $V_{gs}$ measurements of JLRFIB.