Spacer Lithography for 3D MOS Devices Using Amorphous Silicon Deposited by ECR-CVD

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The spacer lithography (SL) is a promising method for the sub-22 nm CMOS (complementary metal-oxide-semiconductor) technology[1]. In this work, hydrogenated amorphous silicon (a-Si:H) films have been deposited by electron cyclotron resonance (ECR) – chemical vapor deposition (CVD) and they used as spacer to implement of the spacer lithography (SL) technique, which is employed to fabricate of the structure of three-dimensional MOS capacitor (3D MOS capacitor). For this, the sequential process steps were carried out (Figure 1): cleaning of Si substrate, thermal oxidation of Si to get a SiO_2 film (thick layer of 10 nm), sputtering deposition of Al (thick layer of 100 nm), optical lithography and wet etching of Al (using H_3PO_4 + HNO_3 solution) to define the Al mesa region, ECR-CVD deposition of a-Si:H (thick layer of 150 nm), Reactive Ion Etching (RIE) to remove a-Si:H layer on Al and on SiO_2, leaving the a-Si:H layer on side wall of Al mesa, wet etching of Al mesa (using H_3PO_4 + HNO_3 solution), Reactive Ion Etching (RIE) to remove a-Si:H spacer, SiO_2 and Si, defining the 3D structures with Silicon Nano-Wires (SiNWs) on Si surface (with widths thinner than 100 nm), dry thermal oxidation on Si surface to get SiO_2 (thick layer of 10 nm) gate dielectric, sputtering deposition of Al (thick layer of 100 nm), optical lithography and wet etching of Al (using H_3PO_4 + HNO_3 solution) to define the Al gate electrode of 3D MOS capacitor, sputtering deposition of Al (thick layer of 100 nm) on Si substrate backside, and sintering in forming gas environment at 450^{o}C for 30 min. Figure 2 presents Si surface topography measured by atomic force microscopy (AFM), after the step of RIE to remove a-Si:H spacer, SiO_2 and Si, defining the 3D structures with SiNWs on Si surface (Figure 1(d)), indicating the presence of SiNWs with heights of 17.7 nm. Figure 3 shows the scanning electron microscopy (SEM) micrograph of the sample surface with fabricated 3D MOS capacitors, indicating the presence of SiNWs and Al gate electrodes. The electrical characterization of the capacitors was obtained by capacitance-voltage (CxV) curves, such as presented in Figure 4, indicating that the capacitors are working, because the accumulation, depletion and inversion regions of carriers in the Si substrate with SiNWs are defined perfectly. Furthermore, the effective charge densities lower than 10^{11} cm^{-2}, extracted from flat-band voltage values (such as -1.1 V) of CxV curves, are acceptable for MOS devices. Thus, from these results, it can be conclude that our spacer lithography method can be used to get 3D MOS devices, such as FinFETs and JunctionLess, which are based on SiNWs.

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[1] L. Chang et al., *P IEEE*, **91**, pp. 1860-1973 (2003).

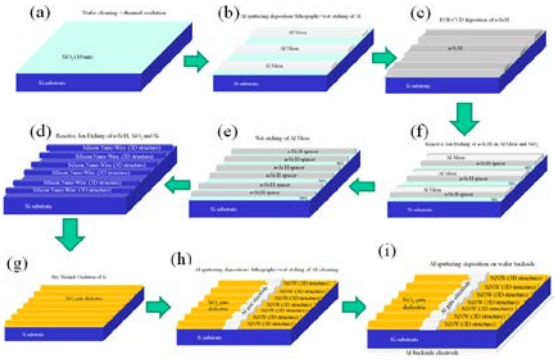

Figure 1: The sequential process steps for 3D MOS capacitors

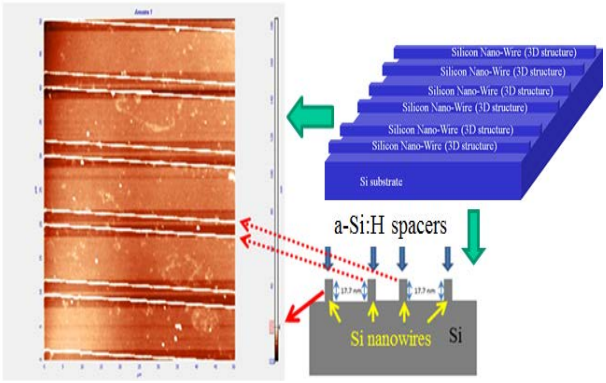

Figure 2: The 2D surface topography of the sample measured by atomic force microscopy (AFM) with the SiNW of 17.7 nm (height) as shown the schema.

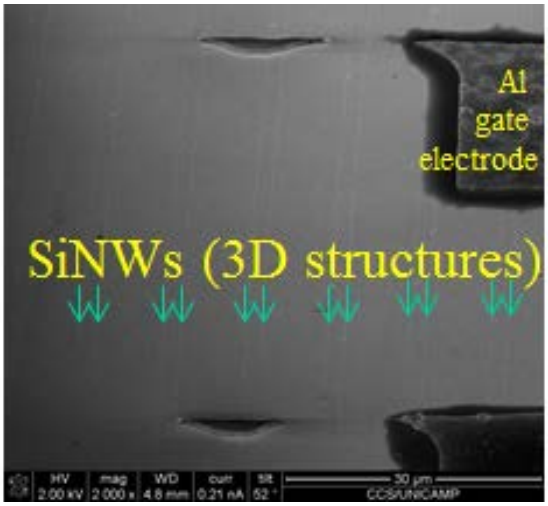

Figure 3: SEM micrograph of the sample surface presents 3D MOS capacitors on SiNWs

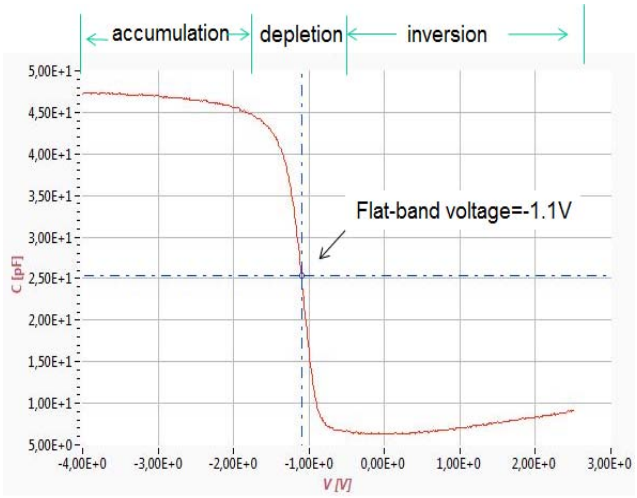

Figure 4: C-V curve of 3D MOS capacitor