Fabrication of silicon nanostructures with large taper angle by reactive ion etching

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In dry plasma etching, two types of profile can result: isotropic (curved sidewall profile) and anisotropic (ideally straight vertical profile), with the later being the most desirable for majority applications. However, tapered profile with large taper angle is needed for some applications such as light trapping in solar cell or CMOS imaging devices. Whereas small taper angle (<10 deg) can be readily achieved by slightly modifying the recipe from the one giving vertical profile, taper angle of >20 deg is challenging and rarely reported in the literature. One method is to use KOH wet etching of silicon that gives a fixed taper angle of 35.3 deg. For dry etching, two approaches have been demonstrated. The first one is to add an isotropic etching step (using SF_6) to the standard Bosch process cycle, which results in a scallop sidewall undesirable for nanoscale etching[1]. The second one relies on the fast lateral etching of the resist (as etching mask) using a recipe that normally gives a vertical profile when a hard mask is used[2].

For silicon etching, many groups have developed recipe with vertical profile capable of ultra-high aspect ratio etching[3,4,5,6]. Here we took the recipe reported in Ref. [3] and shown in Table 1 as the starting point. One can generally obtain tapered profile by promoting inhibitor (here fluorocarbon polymer) formation and decreasing its removal rate, which in turn could be realized by increasing the ratio of C_4F_8/SF_6, reducing the RF bias power, and/or increasing the gas pressure. Figure 1 shows the etching profile after drastically reducing the C_4F_8/SF_6 ratio from the baseline value of 38/22 to 59/1 (the total gas flow was fixed at 60 sccm), which gave a sidewall taper angle of 22 deg. As expected, the etching rate dropped from 400 nm/min to 32 nm/min. As it is not possible to further reduce the gas flow ratio, we reduced the RF bias power from 20 W to 10 W, which led to a taper angle of 39 deg (figure 2), higher than achieved by KOH etching of silicon (35.3 deg). The etching rate was further decreased to 15 nm/min. However, due to excess inhibitor formation, the etched surface was rough that could be advantageous for light trapping application. Further reducing the RF bias power to 5 W led to negligible etching of silicon (not shown).

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C4F8 (sccm)	SF6 (sccm)	RF power (W)	ICP power (W)	Pressure (mTorr)	Si etch rate (nm/min)
38	22	20	1200	10	400

Table 1. Baseline recipe that gives a nearly perfect vertical profile using Oxford ICP-RIE (ICP 380). The total gas flow is 60 sccm.

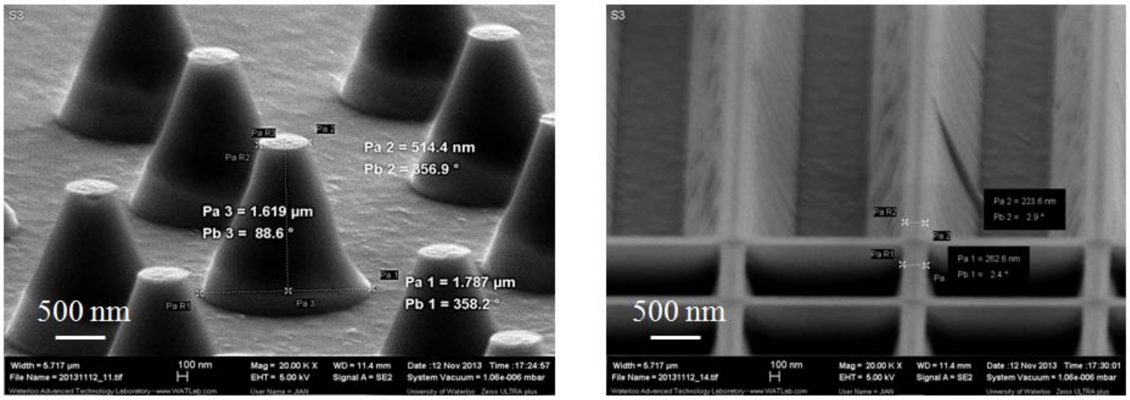

Figure 1. SEM images of silicon structures etched with C_4F_8/SF_6=59/1 (the other parameters are the same as shown in Table 1) for 50 min. The sidewall taper angle is calculated as 22 deg.

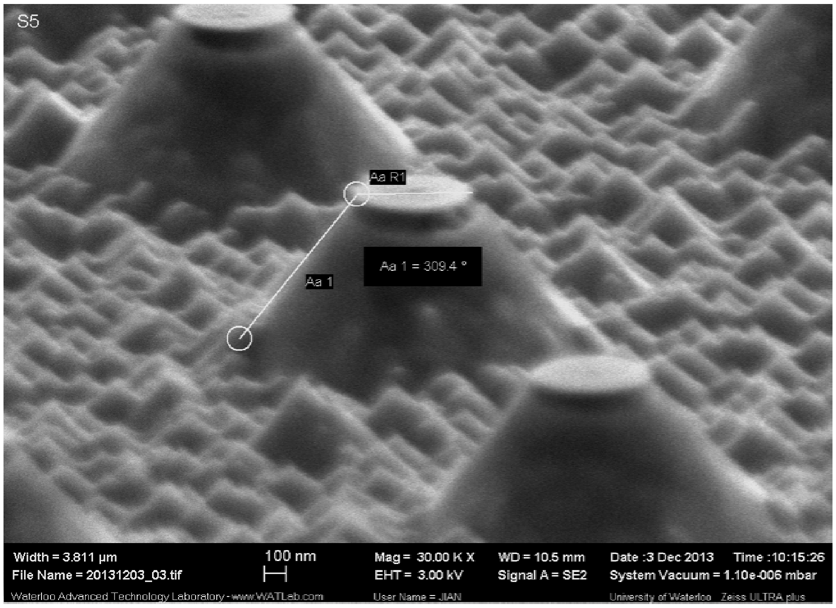

Figure 2. SEM image of silicon structures etched with RF bias power=10W, C_4F_8/SF_6=59/1 for 50 min. The sidewall taper angle is 39 deg.