Study on the correlation of Hole etch and Byproduct

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The hole etch process of DRAM uses the multi step process not to be interfered by byproduct. The hole becomes smaller and deeper as design rule gets smaller, so byproduct interference increases more and more.

There are still a lot of problems to be solved in DRAM products. For example the hole bottom unetch, the bad disperse of hole size.

We had studied the optimized conditions by hole size to improve the hole size disperse and the bottom etch ability. The result of that will be described in this paper.

1. Introduction

Memory Device has progressed to reduced the Design Rule(D/R). As Design Rule get smaller, contact hole etch is more difficult. So Dry Cleaner has been used.

Dry Cleaner has the property that form byproduct. Byproduct is interfering gas reaction. Therefore there is a saturation amount in Dry Cleaner Etching. [Figure.1] So Multi Cycle has been used.

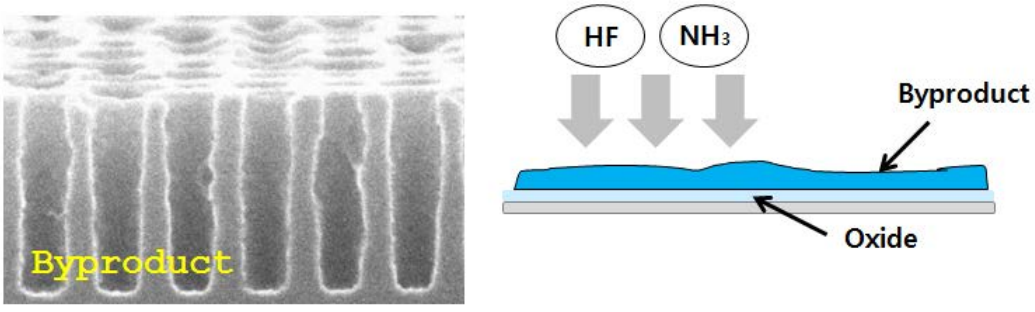

Figure.1 : Dry Cleaner Etching Characteristic

As Design Rule get smaller, a lot of problems has occured, such as Hole Bottom unetch, bad CD disperse.[Figure.2]

Accordingly, a method to solve these problems is required.

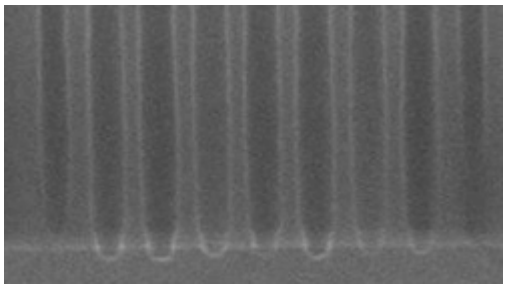

Figure.2 : Failure of bottom unetch

2. Main Discourse

2.1 Concept of experimental : STC(Stepwise Time Control)

This feature allows you to minimize the interference of the byproduct using the stepwise time application to each Cycle(Hole Size).
This concept is to decrease the time first cycle, and offset the missing time later. [Figure.3]

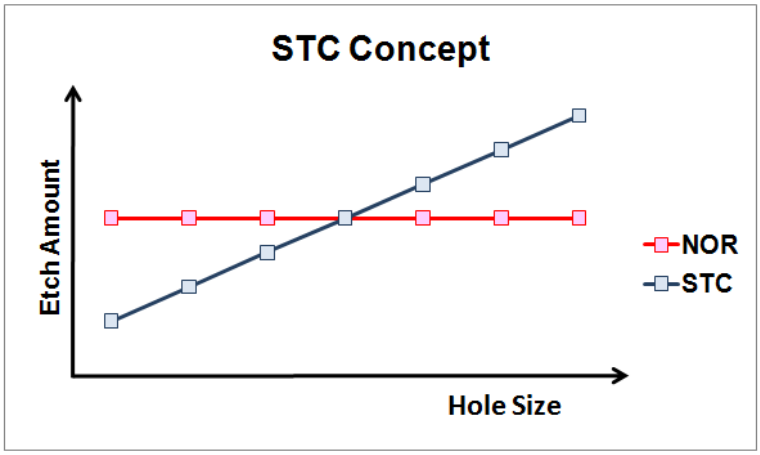

Figure.3 : STC(Stepwise Time Control) Concept

2.2 Evaluation of the experimental

- The purpose of the experiment : Derivation of the optimal stepwise value in relation to the Byproduct and Hole Size.
- Test sample : 26nm Hole Pattern
- Test condition : 7Cycle Enlarge (20” base)
- Test Result : Stepwise Value = 1~3” [Figure.4]

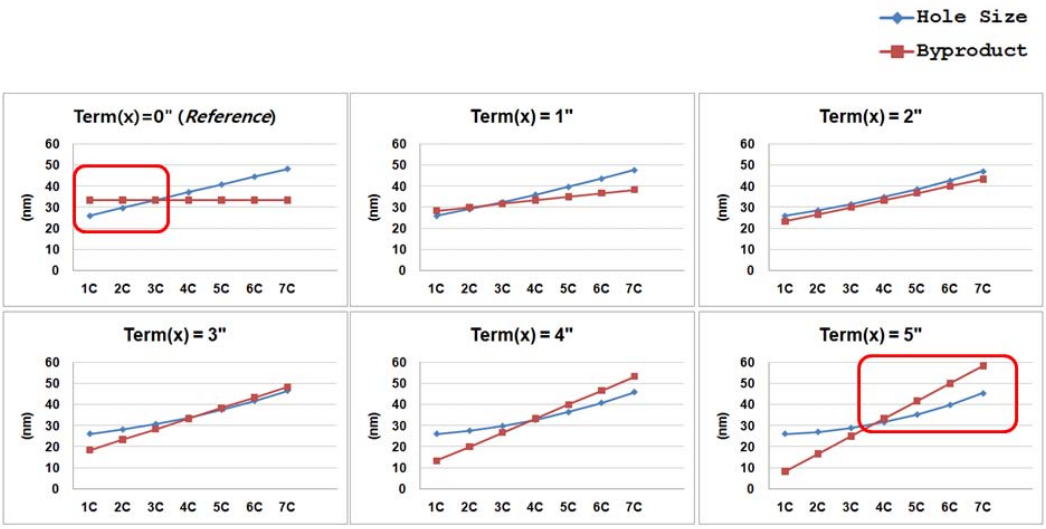

Figure.4 : Correlation between the Byproduct and Hole Size by STC value

2.4 Formal derivation

$$Holesize > Byproduct$$

$$C_1: \frac{HoleSize}{2} \times \frac{1}{(Byproduct-1)} > (Basetime-3x) \times Etchrate$$

$$C_2: \frac{C_0 HoleSize}{2} \times \frac{1}{(Byproduct-1)} > (Basetime-2x) \times Etchrate$$

$$C_3: \frac{C_1 HoleSize}{2} \times \frac{1}{(Byproduct-1)} > (Basetime-x) \times Etchrate$$

$$\vdots$$

$$C_7: \frac{C_5 HoleSize}{2} \times \frac{1}{(Byproduct-1)} > (Basetime+3x) \times Etchrate$$

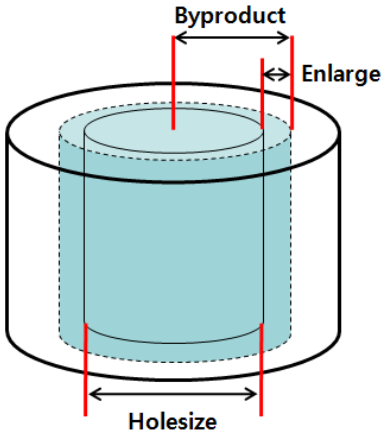

Figure.5 : STC(Stepwise Time Control) Formulation

● STC Formula

$$\frac{1}{C-1}\left(2t_0 - \frac{d}{(B-1)r}\right) < x < \frac{1}{B(C-1)}\left(2t_0(C-B) + \frac{d}{r}\right)$$

$d : Holesize\,(nm)$
$B : Byproduct\,(times)$
$t_0 : Basetime\,(s)$
$r : Etchrate\,(nm)$
$C : Cycle$

3. Conclusion

As Design Rule get smaller, the smaller, deeper and more difficult the contact becomes.

Optimal etching time to each Hole Size that was proven in this paper, will be a contribute to form the proper shape without loss. Further, it can be widely applied in the next generation products.

4. Reference

[1] Mongsup.Lee, Contact Enlarge by Using Dry Cleaning.
[2] Chun Su Lee, Modeling and Characterization of Gas Phase Etching of Thermal oxide and TEOS Oxide Using Anhydrous HF and CH3OH.
[3] M. Saadoun, Formation of luminescent (NH4)2SiF6 phase from vapor etching-based porous silicon