Roughness mitigation techniques for electron beam lithography

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ABSTRACT

With the constant down-scaling of features in the semiconductor industry, Line Width Roughness (LWR) is considered as the factor limiting the miniaturization. In recent years, several papers showed the importance of LWR reduction in order to meet the ITRS[a] requirements for the sub-22nm technological node (sub-2nm LWR). This topic is well documented for Extreme Ultra Violet (EUV) lithography, which is currently the most mature next-generation lithography (NGL) technique. In this article, we assess the capability of ebeam/multibeam lithography, which remains a serious competitor for NGL, to print 32 nm half-pitch line and space resist patterns with the lowest LWR. We propose several strategies including writing strategies and introduction of underlayers, to reduce resist pattern LWR. We also investigate the effect of post-lithography treatments to mitigate the resist LWR. Finally, the transfer of the reduced resist pattern LWR is evaluated during the subsequent plasma etching processes involved in the gate stack patterning.

All the exposures of this study are made with a Vistec shaped-beam tool SB3054DW with an acceleration voltage of 50kV. The resist used is the current reference resist (positive CAR) designed for the 5kV multi-beam lithography Mapper prototype equipment (Asterix). The plasma etching transfer into the gate stack is performed in a DPS II Centura 300 inductively coupled plasma etch tool from Applied Materials. The final objective is to transfer the complete protocol developed on 50kV exposures to 5kV multi-beam exposures. All the LWR measurements are made with a Hitachi CDSEM HCG4000 and a power spectrum density fitting method is used to obtain unbiased values of LWR[b] as well as spectral information on the LWR.

The experimental results show the effectiveness of writing strategy using biased patterns to decrease the resist pattern LWR (cf. Fig.1). Various post-lithography processes (such as thermal processing, plasma treatments, and in-track surfactant rinse) already developed for 193-nm methacrylate based photoresists[c] were tested on the ebeam resist used in this study (cf. Fig.2). Surprisingly, plasma treatments such as HBr or H_2 plasmas that were very efficient to decrease 193nm PR pattern LWR[d],[e] have no significant impact on this ebeam resist. In our case, thermal processing is the most promising post lithography treatment with a 20% LWR decrease. Other post-lithography treatments combining several strategies together are under investigation to push further the limit of ebeam resist LWR mitigation.

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[e] Proc. SPIE 8328, Advanced Etch Technology for Nanopatterning, 83280L (March 29, 2012).

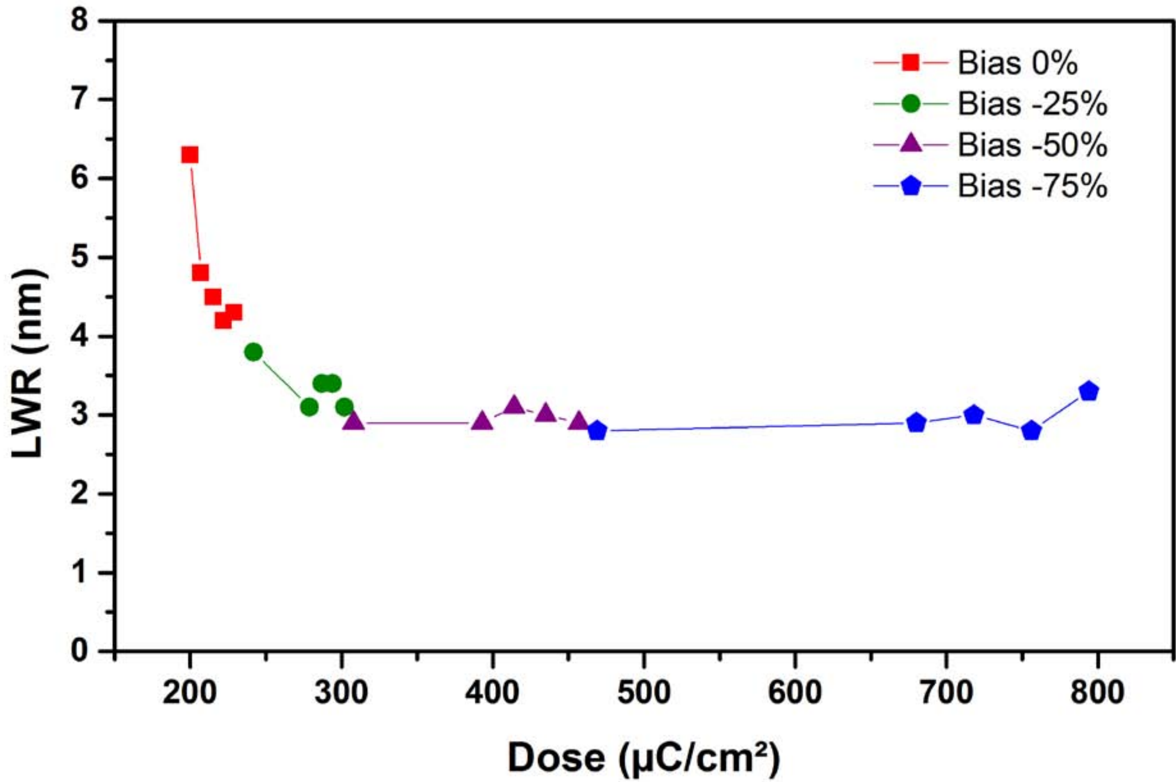

Fig. 1: Effect of biased designs on resist LWR (exposure area is reduced by 25%, 50% and 75% respectively for biases -25%, -50% and -75%)

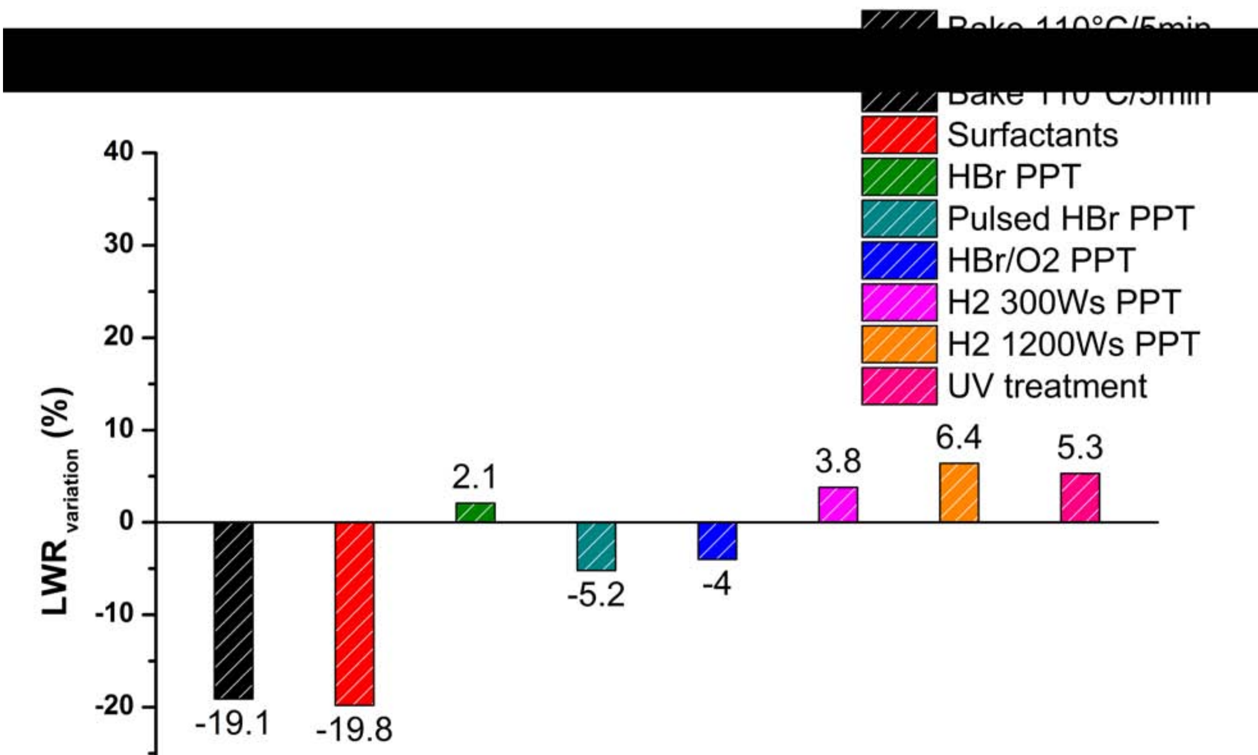

Fig. 2: Effect of post-litho treatments on resist LWR