# Optimizing $SiO_2$ Hard Etch Masks for Atomic Scale Patterning

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Patterning and subsequent oxidation at the atomic scale on silicon presents a vast opportunity to etch and fabricate novel sub-5 nm sized three dimensional structures. However, significant experimental challenges are present in both silicon oxidation and the etch process for patterns smaller than 10 nm. The quality of the oxide can substantially influence the etch characteristics. Over the last two years we have advanced our ambient AFM oxidation lithography and subsequent etch processes to result in sub-10 nm etched features. However, extending the process to the atomic or single nanometer scale using H-based STM lithography and *in situ* post-patterning oxidation enables robust creation of nanometer sized oxidized patterns. However the nature of the oxide formed in the post-patterned oxidation process may be substantially different than the oxide chemistry that results from the field driven oxidation process when doing conductive AFM in air. It is essential to understand the dynamics of the formation of the silicon / oxide interface and the chemical nature of the oxide.

In this paper we will evaluate 1 to 10 nm sized patterns fabricated using SPM lithography of H-passivated silicon surfaces prepared in a UHV environment. The process involves thermal annealing of silicon 100 substrates with previously patterned fiducial marks that facilitates access to atomic scale structures in external instrumentation. The surface is then passivated with atomic hydrogen and an STM probe is used to create atomic scale patterns by selectively desorbing H atoms from the hydrogen passivated surface. New results will be presented using post-patterning oxidation methods that result in oxidation of only those exposed Si atoms. Specialized low temperature oxidation processes and thermal budget control strategies are being developed to grow robust oxide layers while preserving the hydrogen lithography mask. We utilize Auger electron spectroscopy and ellipsometry to characterize and model the underlying mechanisms of the oxidation process to obtain robust patterns that can withstand state of the art etch processes. Low energy RIE and low energy electron enhanced etching are used to transfer the nanometer scale oxidized STM patterns into the Si.