Transfer-Free Wafer-Scale Growth of Graphene on Thin-Film Copper

M.A. Cullinan
Dept. of Mechanical Engineering, University of Texas at Austin, Austin, TX 78712
michael.cullinan@austin.utexas.edu

G. Cheng, B. Sperling, A.R. Hight Walker, A. Davydov, and J.J. Gorman
National Institute of Standards and Technology, Gaithersburg, MD, 20899
gorman@nist.gov

Graphene has received considerable attention over the last decade due to its exceptional electrical, mechanical, and optical properties for applications including high-speed transistors and electromechanical mass sensors. As a result, there is significant interest in the development of graphene growth processes that can be easily integrated into standard process flows. The dominant approach for wafer-scale fabrication uses chemical vapor deposition (CVD) to grow graphene on Cu foils, which is then transferred to a process wafer using a supporting polymer layer. This transfer step can introduce stresses and defects into the graphene, as well as impurities from the chemicals used, which can reduce the quality and repeatability of the resulting devices. More recently, direct CVD growth on thin-film Cu located on the process wafer has been demonstrated [1] and the material quality has been analyzed for a limited set of growth and material conditions [2]. In this paper, an extensive study on CVD growth of graphene on thin-film Cu is presented with an emphasis on the resulting graphene quality as a function of the growth temperature and run time, the Cu film thickness, and the thickness of the Ni adhesion layer between the Cu layer and the silicon dioxide substrate.

One of the biggest challenges in growing graphene on thin-film Cu is that holes can form at the interfaces between grain boundaries in the Cu film due to capillary forces which act to reduce the free energy of the film interface (Fig. 1a) [3]. However, our results show that these holes can be avoided if: 1) the Ni adhesion layer between the Cu film and silicon dioxide substrate is at least 50 nm thick, 2) the Cu film is at least 500 nm thick, and 3) both films are evaporated rather than sputtered. Under these conditions, the resulting graphene is of high quality as determined by Raman spectroscopy (Fig. 2). In particular, the film has a very low defect density (the *D* peak is barely detectable) and is uniformly single layer (the I_{2D}/I_G ratio is between 2.25 and 2.6, which is close to that found for graphene grown on Cu foil). This process has been used to fabricate graphene membranes suspended by Au contacts, as shown in Fig. 3, in which the Cu film is used as a sacrificial layer. Additionally, metal interconnects have been embedded within the silicon dioxide layer for integrated devices including transistors and resonators.

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[2] C.A. Howsare, X. Weng, V. Bojan, D. Snyder, and J.A. Robinson, *Nanotechnology* **23** 135601 (2012).
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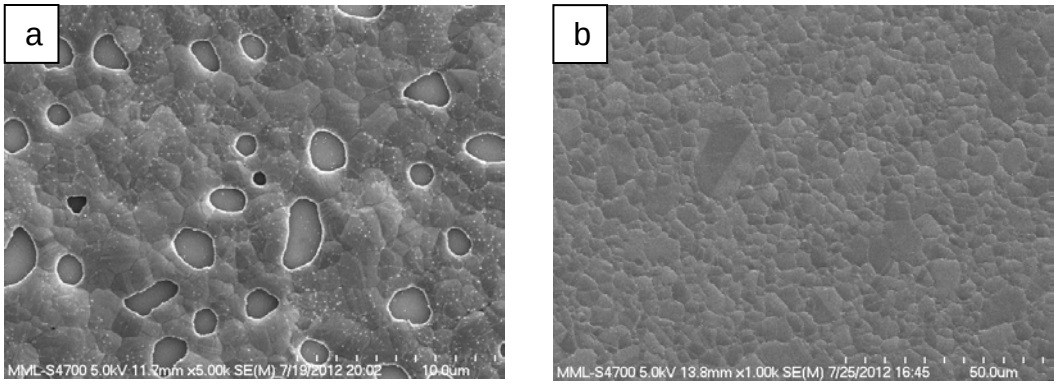

Figure 1: Hole formation in sputtered copper thin films. a) 500 nm thick Cu film with graphene showing holes, b) 750 nm thick Cu thin film with graphene without holes. Both samples were grown at 1000°C.

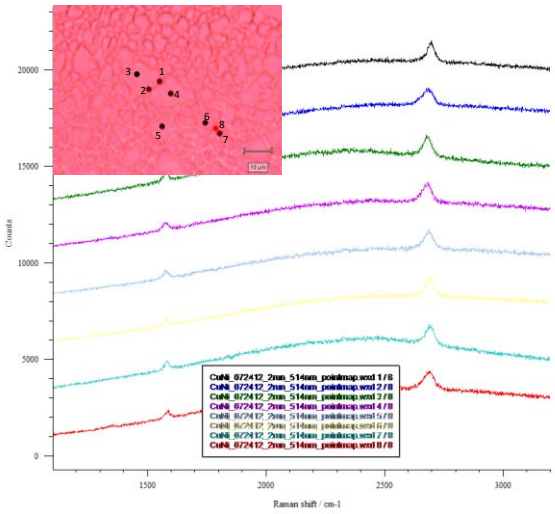

Figure 2: Raman spectra of graphene at various locations on a 1 µm thick Cu thin film. Inset: Optical image of graphene/Cu sample showing measurement locations.

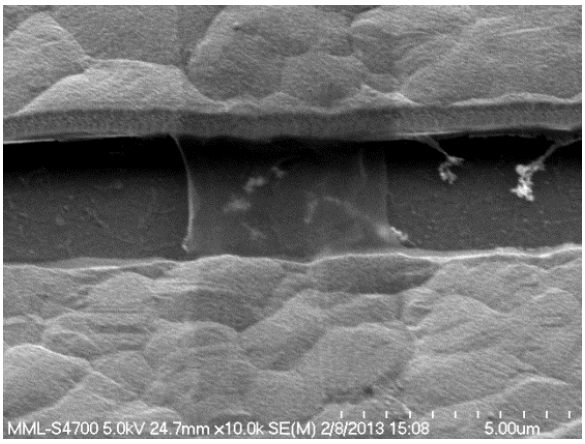

Figure 3: A released single layer graphene bridge suspended between Au contacts.