Proposed Architecture of a Multi-Column Electron-Beam Wafer Inspection System for High Volume Manufacturing

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While optical patterned wafer inspection systems have been successfully used for many years to both improve and control yield during wafer fabrication, their sensitivity is no longer adequate to meet advanced device manufacturing requirements.^{1,2} An alternative is to use wafer inspection systems based on electron-beam technology, which have been commercially available for many years.³ However, the relatively low throughput of these single beam systems has kept them from being used to support high volume manufacturing. Their low throughput is predominately due to two sources. The first is bandwidth limitations inherent in the SEM architecture, and the second is Coulomb repulsion effects in the electron beam.⁴ Both of these sources are complex and have many interdependencies, but they have been optimized to a high degree in commercial systems and further improvements are likely to be incremental.⁵

An obvious way around this would be to use multiple columns. However, it has proven difficult in the past to build columns small enough to fit many on a 300mm wafer and also have the performance of a large single column. Recently, a commercially available SEM that utilizes a miniature field-emission column was shown to have adequate resolution to locate defects in a test pattern provided by SEMATECH [Fig. 1]. The column is all electrostatic and the lenses and deflectors are made of silicon using MEMS techniques.⁶ This technology can be used to build very small columns optimized for the high speed and high current requirements of electron beam inspection. Fig. 2 shows the relative size of the present commercial column and the proposed inspection column, while Fig. 3 shows a possible array arrangement of the small columns.

We will cover the specialized requirements and tradeoffs for multi-column electron-beam wafer inspection, the design requirements for the small inspection columns, and the expected performance of such a system.

¹ Yield Enhancement, Int. Technol. Roadmap for Semiconductors (2013)

² B. Thiel, *et al.*, Proc. SPIE 9236, (2014)

³ D. Hendricks, *et al.*, Proc. SPIE 2439, 174 (1995)

⁴ A. D. Brodie, *et al.*, Microelectronics Engineering, Vol. 17, 399 (1992)

⁵ W. D. Meisburger, *et al.*, J. Vac. Technol. B 10(6), 2804 (1992)

⁶ J. P. Spallas, *et al.*, Microelectron. Eng. 83, 984 – 989 (2006)

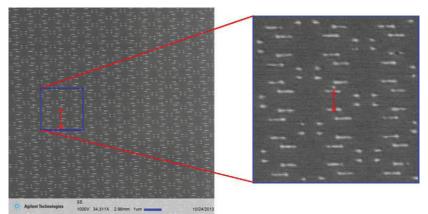


Figure 1: Defect in a SEMATECH provided 22nm test structure imaged by a miniature column SEM (Keysight 8500A)

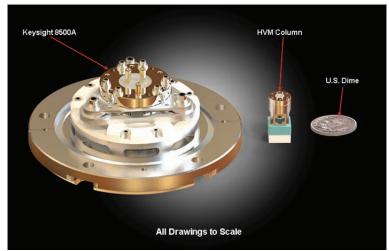


Figure 2: Size comparison of commercial miniature column and proposed inspection column

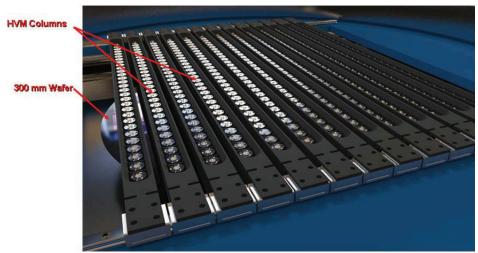


Figure 3: Array of inspection columns arranged over a 300mm wafer