Electrical Yield Verification of Half Pitch 15 nm Patterns using Directed Self-assembly of PS-*b*-PMMA

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Directed self-assembly (DSA) lithography has been expected to become one of the most promising next generation lithography candidates for half pitch (HP) sub-15 nm patterning. There have ever been reported several HP sub-15nm patterning processes with polystyrene-*block*-poly(methyl methacrylate) (PS-*b*-PMMA) lamellar block copolymer (BCP) such as lift-off flow[1], LiNe flow[2] and SMART^{TM} flow[3]. We have also proposed a novel HP sub-15 nm patterning process with low cost of ownership (COO), "coordinated line epitaxy (COOL) process", which requires neither special pinning guide materials to control surface free energy nor resist strip process after guide line pattern fabrication[4, 5].

In order to carry out our process verification across 300 mm wafer for practical semiconductor device manufacturing, we demonstrated an electrical open and short yield test using the "COOL process" for HP 15 nm patterning with PS-*b*-PMMA, as shown in Fig. 1. The electrical open and short yield test could reveal our process viability from the perspective of total practical performance including critical dimension (CD) control, defect control, positioning error, line edge roughness (LER), line width roughness (LWR), and process window in pattern transfer process.

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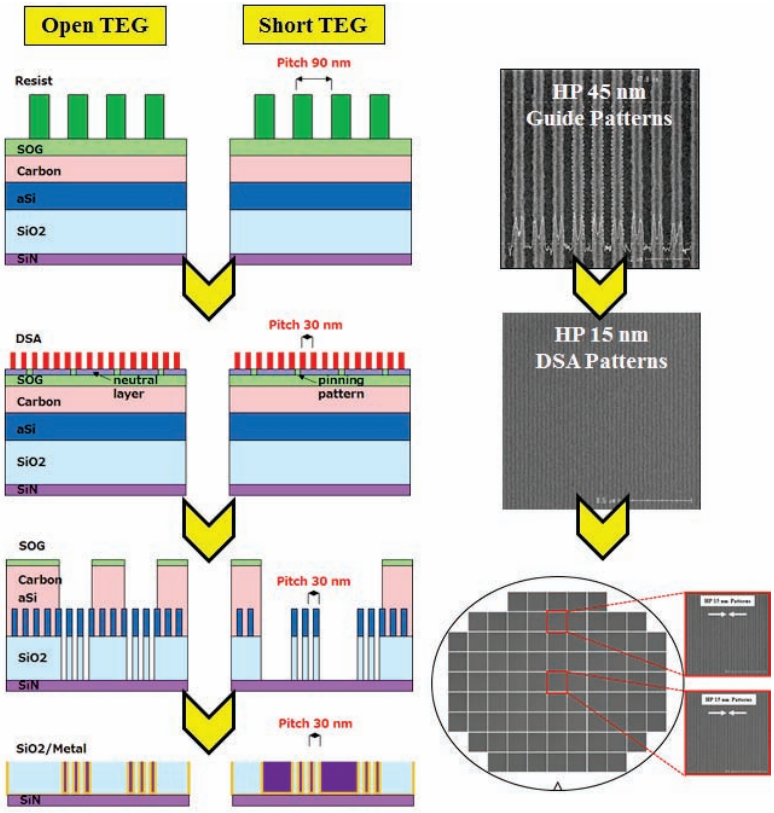

Figure 1. Electrical open and short yield test using "COOL process" for HP 15 nm patterning with PS-*b*-PMMA across 300 mm wafer.