Directed Self-Assembly Process Integration – Fin Patterning Approaches and Challenges

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Introduction:

It has become increasingly complicated and expensive to further minimize feature dimensions as required to push the limits of Moore's law since resolution requirements for photolithography have reached beyond the wavelength of light. Insertion timing of EUV lithography for High Volume Manufacturing is still uncertainty due to source power and EUV mask infrastructure limitations.

Several approaches for pitch division is being employed to extend the limits of 193nm immersion lithography such as Double Patterning Pitch Division (DPPD), and/or Spacer Based Pitch Division (SBPD) schemes (e.g. Hard mask image transfer methods (Double, Triple, Quadruple)). However there is an associated risk/compromise of process complexity, and overlay accuracy budget.

Directed Self Assembly (DSA) offer the promise of providing alternative ways to extend optical lithography cost-effectively for sub-10nm nodes and present itself as an alternative pitch division approach. As a result, DSA has gained increased momentum in recent years, as a means for extending optical lithography past its current limits. The availability of a DSA processing line can enable to further push the limits of 193nm immersion lithography and overcome some of the critical concerns for EUV lithography.

Robust etch transfer of DSA patterns into commonly used device integration materials such as silicon, silicon nitride, and silicon dioxide had been previously demonstrated [1,2]. However DSA integration to CMOS process flows, including cut/keep structures to form fin arrays, is yet to be demonstrated on relevant film stacks (front-end-of-line device integration such as hard mask stacks, and STI stacks). Such a demonstration will confirm and reinforce its viability as a candidate for sub-10nm technology nodes.

In this contribution, we will present/propose fin patterning approaches and challenges for sub-10 nm CMOS technology nodes, which includes demonstration of DSA integration to CMOS process flows with front-end-of-line device film stacks.