Exploring Neon GFIS Nano-Machining Applications in Circuit Edit

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Circuit edit (CE) has been a critical step in Intel's product debug cycle since 1989. Focused Ion Beam (FIB) systems are used in circuit edit to complete a series of complex micro and nano machining activities to modify the active device layers in an integrated circuit (IC). FIB CE applications in removing blocking bugs, validating logic and speed path engineering change orders (ECO), validating logic errors, and generating engineering samples help to shorten the product debug cycle and reduce the overall product cost.

Evolution of the IC process technology continues to increase the challenge of circuit edit with smaller critical device dimensions, thinner process layers, densely packed structures, and complex device routing and design architecture.

A noble gas field ionization source (GFIS) based FIB system provides unique opportunities in high-resolution imaging and nano-patterning applications. The ranges of the atomic mass of the ion species (He^+ and Ne^+), ion beam energies (10-35 keV), and high secondary electron yield (SEY) unique in the GFIS source open up a brand new operating window for femto-amp range CE nanomachining applications. This level of high signal-to-noise ratio (SNR) and nanomachining controllability are not attainable using a traditional Ga^+ Liquid Metal Ion Source (LMIS) based FIB systems. However, the characteristics of He^+, Ne^+ and the source technology also pose certain limitations on their applications.

In this paper, the general approach employed, challenges encountered, and early results acquired in neon application development using Zeiss NanoFAB (noble GFIS) platform for circuit edit will be presented. The merits and limitations of applying a Ne^+ beam in high precision circuit edit applications will be shared with the audience.

As an example, the Ne^+ beam patterning bandwidth, artifacts, and limitations were tested and analyzed in great detail on the NanoFAB platform. Figure 1 shows an array of structures patterned by a 10 keV Ne^+ beam under different beam patterning and blanking conditions. This learning enabled a suitable patterning recipe to be selected and applied to a precision milling application. In Fig. 2, a neon beam was used to machine a trench through Si and stop on transistor diffusion fins and poly (metal-gate) regions from the backside of a 22 nm device. The top down endpoint image of neon was correlated and compared with its layout in Fig. 2.

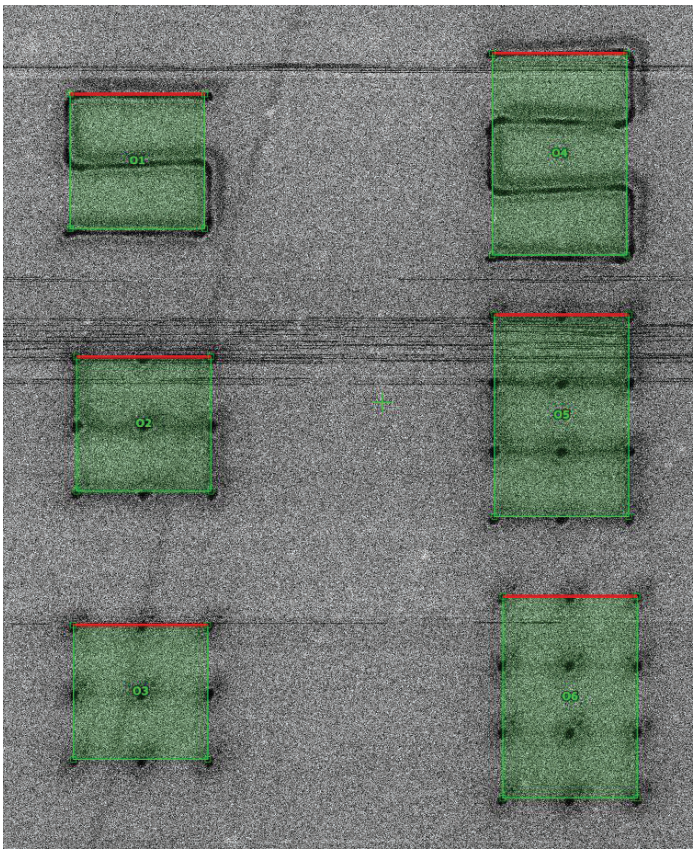

Figure 1: Neon patterning optimized under various beam patterning conditions, including: beam scanning direction, dwell time, and minimizing blanking artifacts.

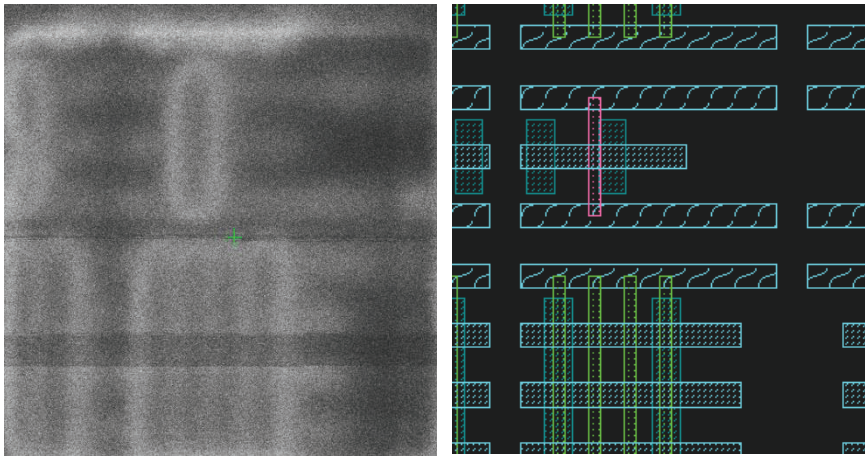

Figure 2: Neon image correlated with device layout.