

# Massively Parallel Silicon Micro-Patterning and Thin Slicing by Magnetically Guided Etching

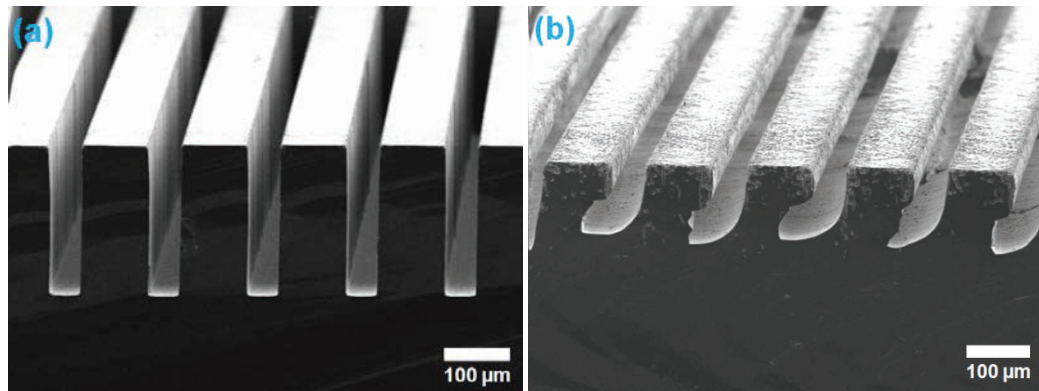
T. K. Kim, D. Chun, C. Choi, C. S. Rustomji, Y. J. Kim, C.-H. Liu, G. Kim, R. Chen, S. Jin

Materials Science and Engineering Program, University of California at San Diego,  
La Jolla, CA 92093

Department of Mechanical and Aerospace Engineering, University of California  
at San Diego, La Jolla, CA 92093

For micro- and nano-patterning and slicing of silicon, electroless etching and shaping can be used for potential applications such as semiconductor devices, energy storage devices, and solar cells. We have successfully developed magnetically guided electroless etching technique for controllable shapes in micro-scale as well as for low-cost slicing of silicon wafers with minimal kerf loss. Various factors affecting such guided Si shaping have been studied, including the electrical resistivity of Si, annealing effect, doping type, etchant composition, magnetic layer structure, and magnetic field intensity.

*n*-type Si wafer with resistivity of 10~30 ohm-cm has higher etching rate than that with resistivity of 1-10 ohm-cm. When Si wafer is annealed in Ar gas after sputtering thin film structure composed of Au and Fe, the etching rate can be increased compared to the as-deposited magnetic layer, which may result from the larger magnetic energy. *p*-type Si forms more porous etched surface and lower etching rate compared to *n*-type Si so that etchant composition consisting of mainly hydrofluoric acid and hydrogen peroxide has to be optimized to decrease the porous structure and increase the etching rate. Two types of magnetic layer structures are fabricated including 3-layer of Fe/Au/Fe and Fe-embedded Au single layer in order to protect the magnetic layer Fe from chemical corrosion by etchant. High-aspect-ratio, vertical micro hole array has also been successfully prepared for possible application in high throughput TSV (Through-Silicon-Via) device fabrication.



*Figure 1: Magnetically guided electroless etching of silicon: (a) Sliced silicon into micro-scaled think layer, and (b) curved micro-patterning of silicon.*