Wafer-Scale Etching of Nanometer-Scale Features With Low Energy Electron Enhanced Etching (LE4)

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Devices with nanometer-scale features promise dramatic improvements in technological performance. Achieving this potential on a commercial scale will require wafer-scale, nanofabrication methods including etching. Systine has developed the Low Energy Electron Enhanced Etching (LE4) technology to address this challenge. The LE4 process operates in a wafer-scale DC plasma platform that has already been scaled up to process 3-inch substrates and can easily be scaled to larger sizes as wafer-scale nano-patterning becomes available. Materials including silicon, oxides, low-k dielectrics, GaAs, GaN and other III-V's have been etched to dimensions much smaller than 10nm with damage-free surfaces that approach atomic smoothness and preserve the stoichiometry.

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Biographical Summary

Stewart has over 40 years of experience in high technology management and consulting at companies including Intel, Cypress Semiconductor, Integrated Device Technology, Hitachi Semiconductor and multiple startups including Systine, Inc. He has worked with products, technologies and intellectual property in the areas of RISC cores, DSP cores, RF and wireless devices, image processing, data compression and encryption, non-periodic signal modulation, carbon nano-materials, excited state surface chemistry and electron enhanced etching. He has a BS Physics and MSEE from the California Institute of Technology and an MBA from the Stanford Graduate School of Business.