Selective Growth and Self-Alignment Requirements for Advanced Patterning Applications

Charles H. Wallace
Intel Corporation, Portland Technology Development, 5200 NE Elam Young Pkwy. Mailstop RA3-355, Hillsboro, OR 97124-6497
charles.h.wallace@intel.com

As feature sizes shrink in semiconductor device manufacturing processes, controlling edge placement error well enough to meet device performance requirements is becoming impossible using conventional patterning techniques. Physical limitations of lithography equipment are routinely pushed beyond their capability which results in lower yields. Scaling of the wavelength of lithography equipment has stalled over the past several generations at 193 nm. The introduction of new lithography methods such as EUV, Imprint or EBDW will improve resolution; however, the issue of edge-placement error will be a problem regardless of the lithography exposure technique. This presentation will discuss past, current and future methods of improving overlay and critical dimension errors using self-alignment and selectivity.

Some major sources of edge-placement errors will be discussed; including overlay, lithography CD variation, line edge roughness, OPC errors, wafer topology and etch bias. Self-aligned processes in logic-product manufacturing reduce edge-placement-errors which improve yield and device performance. Self-aligned VIAs, self-aligned double patterning (SADP) and directed self-assembly (DSA) are some recent examples of complementary patterning techniques to conventional lithography. These processes enable scaling beyond the resolution limits of conventional lithography. In addition to addressing fundamental physical limitations of lithography, these techniques can help to reduce costs because of shorter patterning process flows and the use less expensive equipment.

The need for intelligent material design, chemical solutions and process selectivity (selective etch, deposition and removal) is evident. Lithography is currently used to define the size and position of all features in semiconductor manufacturing. Future lithography processes and techniques will be used to select, activate or remove predefined features. The edge placement of the physical features on the devices will be determined selectively through the use of chemistry, plasma etch selectivity, directed self assembly and/or selective deposition processes. The engineering challenge is how to combine lithography and selective methods together in a high yield, efficient and defect-free manufacturing process flow.