Encapsulated Delamination Transfer and Nanofabrication of Silicene Field-Effect Transistors

Li Tao,^{1,*} Eugenio Cinquanta,² Carlo Grazianetti,² Alessandro Molle² and Deji Akinwande^{1,*} ¹Microelectronic Research Center, The University of Texas at Austin, TX 78758, U.S.A. ²Laboratorio MDM, IMM-CNR,via C. Olivetti 2, Agrate Brianza, I-20864, Italy * tao@utexas.edu; deji@ece.utexas.edu

Silicene, a silicon analogue of graphene, has a buckled honeycomb lattice. Owing to its predicted Dirac band structure¹ and sensitive surface, where external fields and surface interactions can be exploited to influence fundamental properties², silicene has the potential to be a widely tunable 2-dimensional (2D) material for future innovative nanoelectronics³. For instance, interesting phenomena such as quantum spin Hall effect⁴, strain-related thermal conductivity⁵ and piezo-magnetism⁶ have been predicted in silicene. Despite the aforementioned exciting theoretical studies and developing epitaxial synthesis of silicene⁷, it is a challenge to fabricate silicene device due to the air-stability issue⁸. Unlike graphene, it is unfeasible to transfer silicene via widely-used wet transfer technique as even Al₂O₃ capped silicene degrades readily if its surface exposed.

Here, we report our recent progress addressing the air-stability issue by a unique growth-transfer-fabrication process (Figure 1): silicene encapsulated delamination with native electrodes (SEDNE). Key innovations in the SEDNE process include: i) epitaxial silicene synthesis on deposited Ag(111) thin films on mica instead of expensive single crystal Ag catalyst substrates, ii) encapsulated delamination sandwich transfer of silicene in between Al₂O₃ capping, and iii) utilizing native Ag film to stabilize silicene and as contact electrodes. The encapsulation of silicene in between Al₂O₃ and Ag not only improves silicene stability (over 2 months in 30 mbar vacuum storage⁹), but also paves the way to successful silicene transfer (Figure 2) for device fabrication. Using Ag/mica also allows substrate recycle compared to standard wet transfer technique that requires full or partial dissolution of the growth substrates. SEDNE process preserves silicene during transfer and device fabrication, and enables a short time window for Ag-removed silicene device studies. As a result, we demonstrated the first silicene field-effect transistor (FET)⁹, corroborating theoretical expectations on ambipolar Dirac charge transport^{1, 10}. Monolayer mixed-phase (4×4 and $\sqrt{13}\times\sqrt{13}$) silicene based FETs exhibit ON/OFF ratio over one order of magnitude (Figure 3). The measured drain current (I_d) response to gate voltage (V_g) and resistance (R)versus override voltage (Vg-VDirac) agree with widely-used diffusive transport model¹¹, which yield extracted mobility $\sim 100 \text{ cm}^2/\text{V-s}$ at residual carrier density of $\sim 3-7 \times 10^9$ cm⁻². This work suggests a promising route to minimizing the risk of degradation during transfer and device fabrication for air-sensitive elemental 2D materials such as phosphorene and germanene. Importantly, the allotropic affinity of silicene with crystalline bulk silicon suggests a more direct path for silicene integration with ubiquitous semiconductor technology.

Reference:

3. De Padova, et al., J. Phys. Condens. Matter 24, 22, 2012.

- 5. Q.-X. Pei, et al., J. Appl. Phys. 114, 3, 2013.
- 6. Y. D. Nelson, et al., J. Phys. Cond. Matter 22, 37, 2010.
- 7. B. Aufray, et al., Appl. Phys. Lett. 96, 18, 2010.
- 8. A. Molle, et al., Adv. Funct. Mater. 23, 35, 2013.
- 9. L. Tao, et al., Nature Nanotechnology, (accepted), 2015. 10. P. Vogt, et al., Phys. Rev. Lett. **108**, 15, 2012.
- 11. S. Kim, et al., Appl. Phys. Lett. **94**, 6, 2009.

^{1.} S. Cahangirov, et al., Phys. Rev. Lett. 102, 23, 2009.

^{2.} Z. Ni, et al., Nano Lett. 12, 1, 2011.

^{4.} C.-C. Liu, et al., Phys. Rev. Lett. 107, 7, 2011.



Figure 1. Schematics of silicene and its synthesis-transfer-fabrication process. **a**) buckled honeycomb lattice structure of silicene and **b**) Silicene Encapsulated Delamination with Native Electrode (SEDNE) process that includes the following key steps: epitaxial growth of silicene on Ag(111) thin film on mica, *in-situ* Al₂O₃ capping, encapsulated delamination transfer of silicene, and native contact electrodes formation to enable back-gated silicene transistors.



Figure 2: Raman characteristics of silicene film: **a**) in comparison with amorphous Si (a-Si) and Si(100) bulk; **b**) before and after our encapsulated delamination transfer with identical signatures indicating intact silicene.

Figure 3. Silicene transistors operating at Room-temperature. **a**) 3D rendering from atomic force microscopy and **b**) scanning electron microscope image of a fabricated silicene transistor. **c**) I_d - V_g and **d**) R versus (V_g - V_{Dirac}) measurements (dots) of a silicene device that displays ambipolar charge transport in a good agreement with the widely-used diffusive model¹¹ (line). Extracted hole and electron mobilities are 99 and 86 cm²/V-s respectively at residual carrier density ~3-7×10⁹ cm⁻², and ON/OFF ratio is ~10×.

d

R(×10⁶ Ω)

2.5

2.0

1.5

1.0

0.5

0.0

-2

0

Vg-VDirac (V)

2