Fabrication of Nanodamascene Metallic Single Electron Transistor

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We present experimental demonstration of metallic single electron transistor (SET) fabricated using a nanodamascene process and atomic layer deposition (ALD) to form a 1nm Al_2O_3 tunnel barrier.

Chemical mechanical polishing (CMP) is used in the subtractive damascene process to eliminate the possible presence of residual metal near the device, which is common after the liftoff used in traditional processes. It also enables self-aligned formation of tunnel junctions. Atomic layer deposition provides precise control of the tunnel barrier formation and significantly expands the choice of materials available for SET fabrication.

The device was fabricated on SiO_2 insulating layer deposited on silicon wafer by plasma enhanced chemical vapor deposition (PECVD). The pattern of island is written in polymethylglutarimide (PMGI) in Vistec EBPG 5000 100 keV electron beam lithography (EBL) system. PMGI has been shown to have a higher contrast than polymethylmethacrylate (PMMA) and can be used as an etch mask due to its higher etch resistance. Ar, C_4F_8, CHF_3, and CF_4 based inductively coupled plasma (ICP) etching is used to transfer the pattern in PMGI to the SiO_2 substrate (Fig. 1a and b). After the etch, Ni is evaporated onto the sample, filling the pit in the oxide, while rest of the substrate is masked by the remaining PMGI (Fig. 1c). AZ 917 MIF developer is used to remove PMGI and lift-off the Ni overburden. Any residual metal is cleared from the SiO_2 field by a CMP step, leaving a planarized trench filled with Ni (Fig. 1d). Next, a perpendicular line to the island trench is written in PMGI during the second EBL to form the source and drain. A similar etch recipe is used to transfer the pattern into the SiO_2 (Fig. 1e and f). PMGI is then removed and 1 nm of Al_2O_3 is deposited by ALD using trimethylaluminum (TMA) and O_2 plasma (Fig. 1g). A blanket Ni is deposited, and using CMP, the Ni on the field is removed, leaving the trenches filled with metal (Fig. 1h, i and j). Figure 2 shows the top view image of the device using scanning electron microscopy (SEM).

Figure 3 shows the charge stability diagram, “Coulomb diamonds”, of the finished device. The charging energy of the fabricated SET is between 0.2-0.3 meV. This is the first fabricated nanodamascene SET showing metallic behavior with well-defined metallic island and tunnel junctions. We estimate that by choosing SiO_2 as tunnel barrier and scaling down the device dimensions, the operating temperature can be scaled up to 77 K.

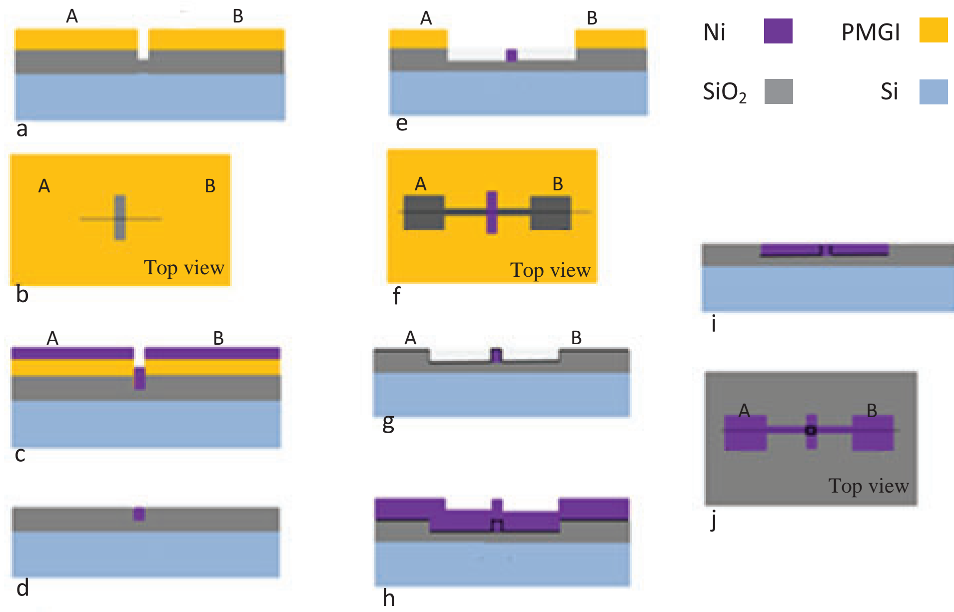

Figure 1. Schematic of the process flow in SET fabrication.

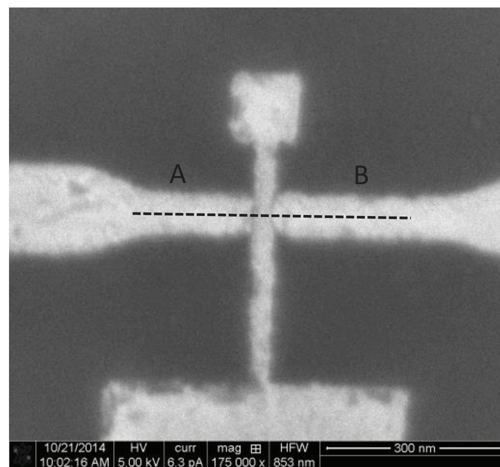

Figure 2. SEM image of the SET.

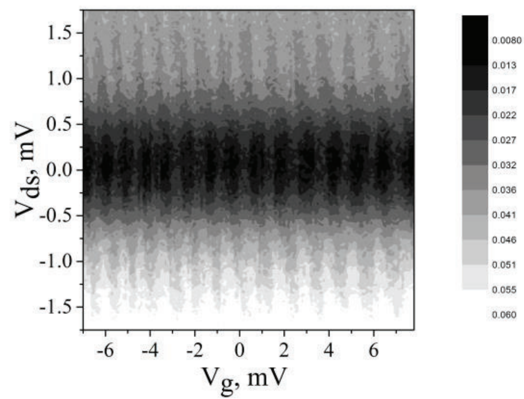

Figure 3. Coulomb diamonds of the SET measured at 1K.