Fabrication of Silicon-on-Insulator Blazed-Grating Optical Couplers using a Thermal Scanning Probe System

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Thermal Scanning Probe Lithography originates from IBM[1] and has recently been commercialized by SwissLitho AG as "NanoFrazor Explore". In 2014, McGill University has acquired the world's first NanoFrazor, and here we present our progress in applying the technology for producing 2D and multilevel 3D surface-corrugated gratings, used as optical fiber-to-chip input/output (I/O) couplers.

Figure 1 illustrates NanoFrazor's cantilever, which has a sharp tip heated with microsecond current pulses that sublimate spin-coated phthalaldehyde (PPA) polymer mask. Holes with better than 10nm of lateral and about 1nm of vertical resolution can be made in the mask resist enabling 3D nano patterns that can be read, and potentially corrected *in-situ*, before transferred into the substrate.

An example of a grating in PPA is shown in Fig. 2(a). Such gratings have been widely used as I/O couplers for silicon-on-insulator (SOI) photonic integrated circuits.[2] However, because of their vertical symmetry, these gratings loose a significant amount of light (around 3dB) to the parasitic substrate radiation. 3D vertically asymmetric blazed gratings and their multistep approximations can provide I/O coupler with sub-dB insertion losses[3] but such devices are difficult to fabricate using conventional lithography techniques. Fig. 2(b) shows a bi-level grating patterned seamlessly with NanoFrazor gray-scale lithography in PPA.

Writing a blazed grating as a bi-level approximation allows for a well-controlled tri-layer pattern transfer[4] to be used, as shown in Fig. 3. In our on-going work, we are using the tri-layer pattern transfer with in-house adopted reactive ion etching (RIE) recipes to transfer the PPA grating patterns in an SOI wafer and demonstrate state-of-the-art performance of the grating I/O couplers.[5]

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[1] P. Vettiger *et al*., IEEE Trans. Nanotechnol. **1**, 39 (2002).
[2] D. Taillaert *et al*., J. J. Appl. Phys. **45**, 6071 (2006).
[3] M. Fan, Ph.D. thesis, Massachusetts Institute of Technology, 2006.
[4] L. L. Cheong *et al*., Nano Lett. **13**, 4485 (2013).
[5] McGill Nanotools Microfab will soon make the tool and the process available to any interested user (http://mnm.physics.mcgill.ca/content/thermal-probe-afm-lithography).

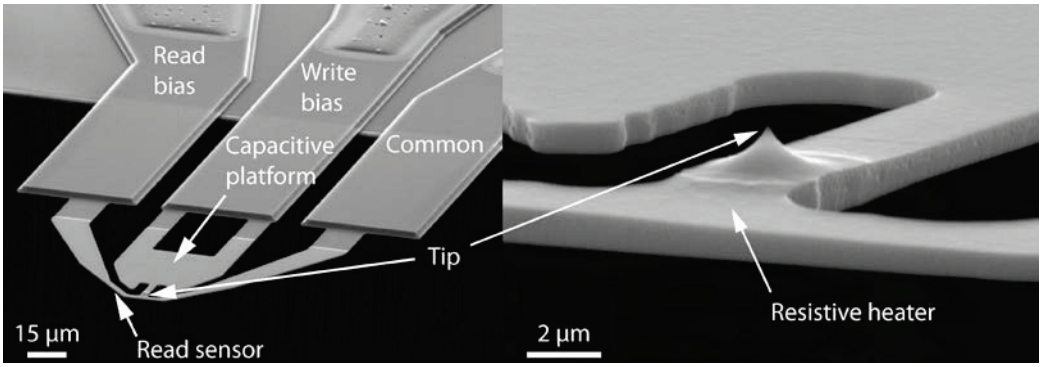

Figure 1: NanoFrazor Cantilever: The micrograph shows a scanning electron microscope image of the NanoFrazor electrostatically actuated silicon cantilever.

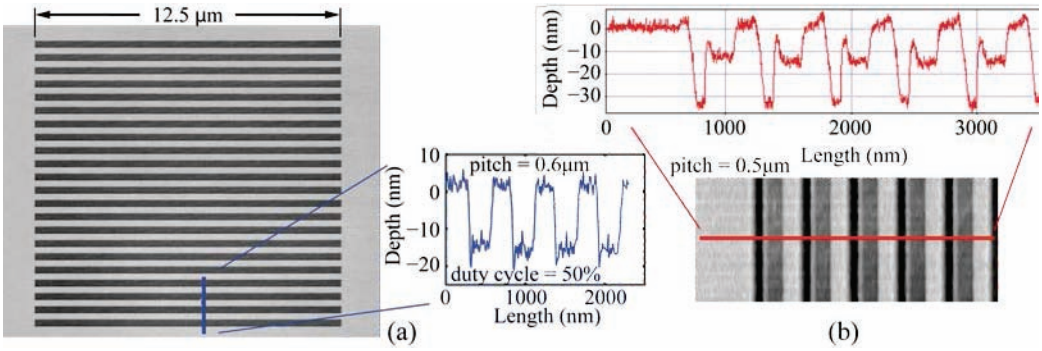

Figure 2: NanoFrazor Patterning of Second-Order Gratings in PPA: (a) regular grating and (b) bi-level grating. Both gratings are patterned and imaged *in-situ* by the NanoFrazor. The bi-level grating is patterned using 5nm pixel size only in the direction perpendicular to the grooves. Otherwise, 20nm pixel size is used for both gratings. At the time of patterning, the tool was between two electronic upgrades and excessive reading noise of ~5nm is superimposed on the grating profiles, as seen in the cross sections. As shown by IBM[4], the typical surface roughness of spin-coated PPA is ~0.3nm (rms), which has also been confirmed by an in-house atomic force microscope.

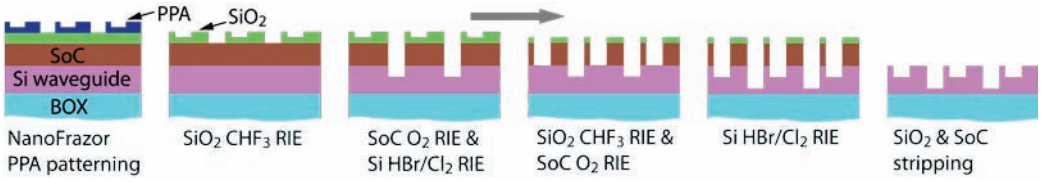

Figure 3: Bi-Level Grating Process Flow: The tri-layer pattern-transfer process[4] requires ~30nm of PPA, ~20nm of SiO_2, and ~50nm of spin-on-carbon (SoC).