Highly Reliable Resistive Switching Devices Based on Tantalum-doped Silicon Oxide

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Memristive or also called resistive switching (RS) devices have attracted extensive interest because of their potential applications in the next generation nonvolatile memory and computing. Silicon oxide is one of the most promising switching materials because it is fully compatible with CMOS [1]. It has been demonstrated that Ni or Pt doped SiO_2 exhibited stable RS, albeit with limited endurance in ambient condition [1, 2]. Here, we reported reliable bipolar RS from Ta-doped SiO_2 with record high endurance ($\sim 3 \times 10^8$ cycles) among SiO_2 based devices. We further adopted a 3-dimensional (3D) vertical structure for our devices, a promising approach to achieve ultra-high bit density [3]. Finally, we studied the scaling of the Ta:SiO_2 devices.

Fig. 1a schematically illustrates the basic device structure with Pt/Ta:SiO_2/Ta geometry fabricated on a SiO_2/Si substrate. 40 nm bottom electrode (Ta) was sputtered onto the substrate, and 3 nm Ta:SiO_2 switching layer was prepared by co-sputtering from Ta and SiO_2 targets. 20 nm Pt top electrode was evaporated through a metal shadow mask. During electrical measurements, Pt electrodes were biased while the Ta electrodes were grounded. A typical IV curve for a device with a 50 μm diameter top electrode is shown in Fig. 1b. The device can be switched ON (low resistance state) at - 0.8 V and OFF (high resistance state) at 1.25 V. The device could be stably switched up to 3×10^8 cycles using 1 μs pulses (- 0.9 V for set and 1.5 V for reset) (Fig. 1c). The resistance was measured at 100 mV between switching events.

Fig. 2a shows the 3D vertical structure for the device. Pt of different thicknesses and 30 nm SiO_2 (as the isolation layer) were sequentially deposited on the substrate using e-beam evaporation and plasma enhanced chemical vapor deposition (PECVD), respectively. Square holes of 50×50 μm^2 were fabricated by photolithography and reactive ion etching with SF_6/Ar that etched through the SiO_2/Pt bilayer and into the SiO_2 substrate. ~ 5 nm Ta-doped SiO_2 was co-sputtered as the switching material, followed by 150 nm thick Ta that was sputtered to refill the holes as top electrodes. During the electrical measurements, Ta top electrodes were biased while Pt bottom electrodes were always grounded. Typical IV curves from vertical devices with different Pt thicknesses were shown in Fig. 2b. The devices exhibited bipolar resistive switching behavior and the operation current decreased with thinner Pt electrodes.

To study the effect of the junction area on the device performance, we fabricated devices with a different 3D structure using 15 nm thick Pt wires with different widths as bottom electrodes and Ta as top electrodes (Fig. 3a and b). Figure 3c shows typical IV curves from devices with different area sizes. The device operation current continuously decreases with smaller devices (Fig. 3d), which can be attributed to the decrease of numbers or dimensions of conductive filaments (CFs).

Multi-layers stacking and electrical characterization on each layer, together with physical characterization on materials and devices will also be presented.

[1]. T. M. Tsai et al. IEEE Electron Device Lett. 33, 1696 (2012).
[2]. B. J. Choi et al. Nano Lett. 13, 3213 (2013).
[3]. S. Yu et al. ACS nano 7, 2320 (2013).

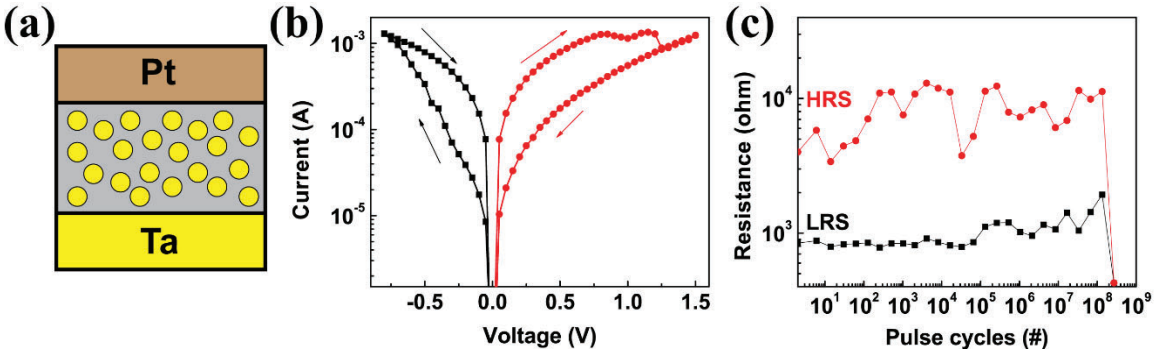

Figure 1. RS in disk-shape devices. (a) Schematic view of device structure. 40 nm Ta and 20 nm Pt are used as BEs and TEs separately, while 3 nm Ta-doped SiO_2 as the switching material is sandwiched in between. (b) Typical bipolar RS IV curves and (c) endurance test (set: -0.9 V, 1 μs; reset: 1.5 V, 1 μs) from devices with a diameter of 50 μm. ~ 3 × 10^8 pulse switching cycles have been achieved.

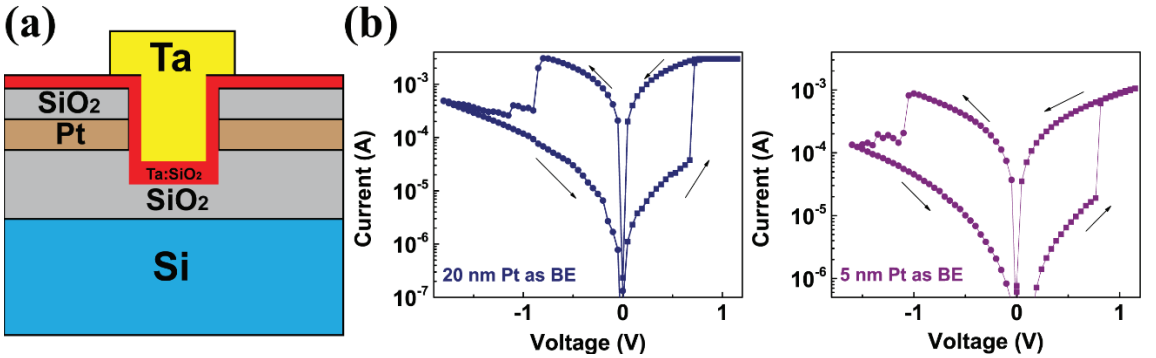

Figure 2. RS from 3D vertical structures. (a) Schematic view of device structure and (b) typical bipolar RS IV curves from devices with different thickness Pt. Similar bipolar RS behaviors are observed while the operation current decreased with thinner Pt electrodes.

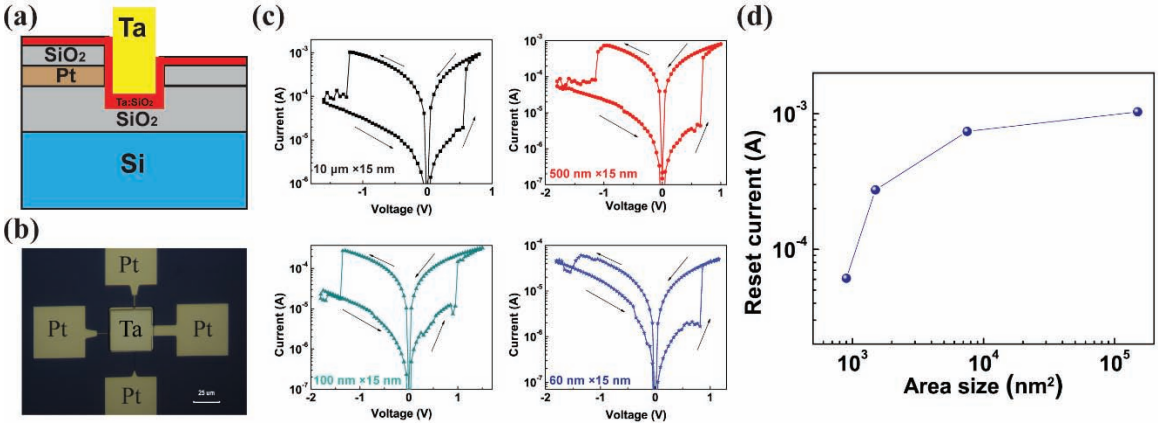

Figure 3. Scaling effect on RS from 3D vertical structures. (a) Schematic view of device cross-section and (b) optical image of the fabricated devices. (c) Typical bipolar RS IV curves from devices with different area sizes. (d) The dependence of reset currents on area sizes. The reset current is defined at where the reset process starts. Scaling down the device will contribute to lower operation current due to fewer or smaller CFs.