Integrated On-Chip Energy Storage Using Porous-Silicon Electrochemical Capacitors

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Integrated on-chip energy storage is increasingly important in the field of *internet of things* and energy harvesting with capacitors being ideal for devices requiring higher powers, low voltages, or thousands of cycles. This work demonstrates electrochemical (EC) capacitors fabricated using porous silicon (P-Si) nanostructures with ultra-high surface-to-volume ratios and an electrolyte.

To maximize the performance, it is important to optimize the pore structure and surface properties. The total surface area needs to be high to obtain large capacitance which requires small pore diameters and deep etch depth resulting in high-aspect-ratio features. Contrariwise for high operating frequency, large pore diameters are preferred for fast ion transport. To optimize these parameters, a tapered-pore nanostructure with main channel sizes tapering from 100 nm to 20 nm (Fig. 1) and ultra-high surface-to-volume ratios was developed (Fig. 2).

Bare P-Si is not stable over a long period of time due to unwanted reactions with the electrolyte, resulting in decreasing capacitance with cycling. Conductive and passivating coatings such as ALD titanium nitride (TiN) or carbon were found necessary for long-term stability. ALD of films in ultrahigh-aspect-ratio features (AR > 100:1) presents unique challenges. To obtain uniform coatings, efficient surface reactions are needed between high volatility, low molecular weight, small molecular diameter precursors without chemical vapor deposition side reactions. The $TiCl_4 + NH_3$ ALD TiN process met these criteria and resulted in passivating conductive films. ALD reactor design also plays a critical role. Whereas the majority of ALD is in a continuous viscous flow reactor, a pseudo stop-flow reactor was used to obtain uniform coatings to a 12 μm pore depth (Fig. 3).

Measurements from the coated P-Si capacitors reveal that high areal capacitance of 3 to 6 mF/cm^2 can be achieved using 2 μm deep pores and 28 mF/cm^2 with 12 μm deep pores, about two orders of magnitude higher than previously reported studies utilizing P-Si.[1,2] Consequently, the energy density of the coated samples is also significantly higher. The P-Si EC capacitors with a TiN coating exhibited a stable capacitance after 1,000 cycles at 50 mV/sec (Fig. 4). The devices were fabricated using silicon process methods with the potential for on-chip integration. The pores can be formed in localized regions on the front side of a Si die or utilizing the backside bulk Si of integrated circuits for kinetic or solar energy harvesting systems such as silicon solar cells[3] or for localized low-energy storage such as for integrated sensors.

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[2] S. Desplobain, G. Gautier, J. Semai, L. Ventura and M. Roy, Phys. Stat. Sol. (c), 4, 2180, 2007.
[3] D.S. Gardner and C. Pint, U.S. Patent #8,816,465, issued Aug. 2014.

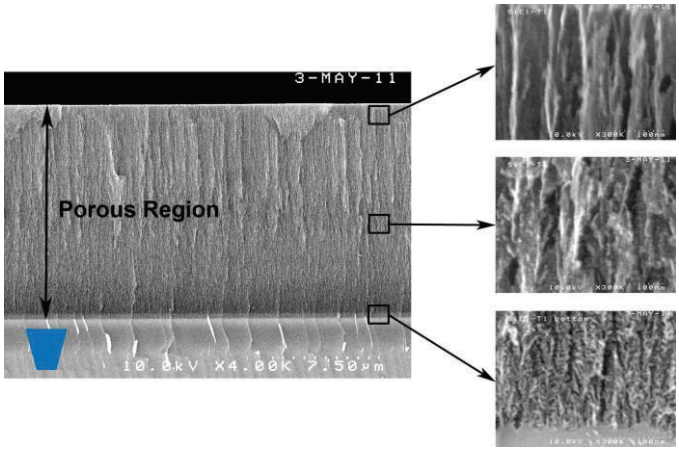

Fig. 1. Tapered porous silicon nanostructure 15 µm deep created by changing the current density during etching. The tapered profile can be optimized for desired device performance (e.g. faster speed or higher capacitance).

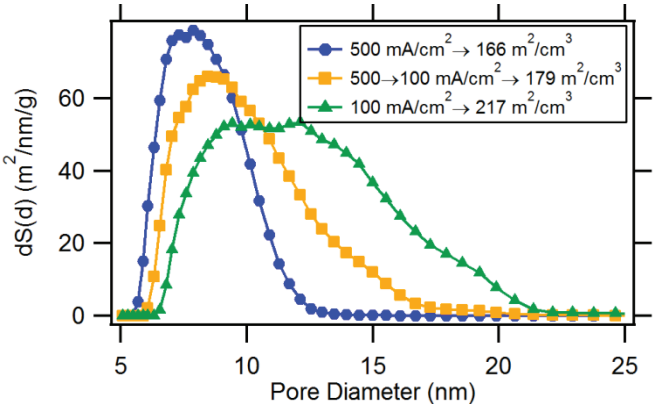

Fig. 1. Pore size distribution from BET absorption analysis of 3 different etching current densities demonstrating the inverse relationship between pore diameter and surface-area density.

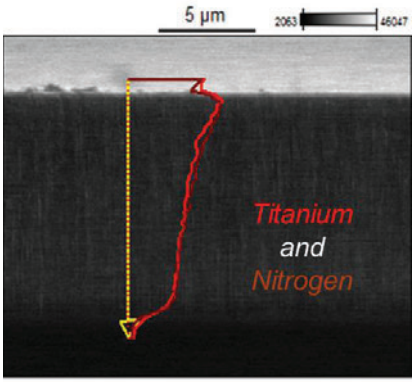

Fig. 3. SEM cross sectional image with an EDS profile superimposed on 12 µm deep pores showing Ti and N concentration as a function of depth.

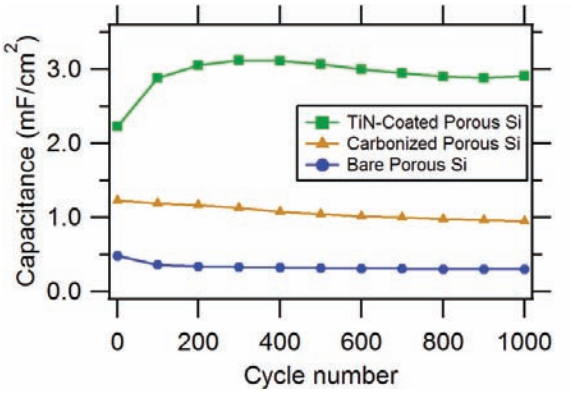

Fig. 4. The capacitance is relatively stable after long term cycling. The areal capacitance density for TiN coated P-Si is 3.1 mF/cm^2 at 0.8 V using 2 µm deep pores.