Quantitative Analysis of Digital STM Lithography Precision

J. H. G. Owen, J. Ballard, U. Fuchs, J. Alexander, C. Delgado, J. N. Randall and J. R. Von Ehr

Zyvex Labs LLC, 1301 N. Plano Rd, Richardson, TX 75081, USA.

jowen@zyvexlabs.com

H depassivation lithography (HDL) using an STM has been used to create dangling bond wires and logic gates,[1] 2-D nanostructures such as dopant based electronic devices,[2] and <6 nm critical dimension 3-D nanostructures[3]—structures whose quality depends upon utmost patterning precision. HDL has the potential to create patterns with a precision limited only by the lattice spacing of the crystal substrate. The patterning process therefore becomes digital, rather than analog, as the precision need not be finer than the atomic spacing.[4]

We have developed a control system to perform automated HDL with a pixel (px) size of one dimer row on the Si(001) surface, which is 7.68Å wide, and is extendable to single atom pixels or other rectangular surface lattices. We use a vector writing approach, in which the tip moves directly to the area to be patterned and writes along vectors whose directions are defined by the surface lattice. Sources of error such as drift and piezo creep are corrected in real time in our controller, in order to allow fast movement without constant reference to the surface lattice, or to fiducial marks. At very large scales, more than about 1 μm, hysteresis effects become significant, and corrections are applied *a priori*.

Comparisons between patterns written with and without real time positioning corrections will be offered. To investigate fine positioning control, we have designed a suite of test patterns, shown below in Fig.1. It is shown that for movements within these fine test patterns, where hysteresis is negligible, positioning errors are reduced by more than 90%, as shown in Fig.2.

On larger structures where precision is critical, the pattern is fractured such that edges are written in the high precision mode, and the bulk filled in using larger spot sizes, which write around 100x faster, but have ill-defined edges. In this way, higher throughput can be obtained while preserving pattern edge precision.[5]

Taking all these elements together, we have developed a set of design rules, which should allow for successful patterning from the single-px to micron scale, allowing fabrication of ultra-precise 2D or 3D structures.

[1] R. A. Wolkow, L. Livadaru, J. Pitters *et al.* “Beyond-CMOS Electronics,” pp. 1–28.

[2] G. Scappucci, G. Capellini, B. Johnston, *et al*. *Nano Lett.* **11** 2272 (2011).

[3] J. B. Ballard, J. H. G. Owen, W. Owen, *et al. J. Vac. Sci. Technol. B,* **32** 041804 (2014).

[4] J. N. Randall, J. B. Ballard, J. W. Lyding, *et al. Microelectron. Eng.*, **87** 955 (2010).

[5] J. B. Ballard, T. W. Sisson, J. H. G. Owen, *et al.J. Vac. Sci. Technol. B* ***31*** 06FC01 (2013).

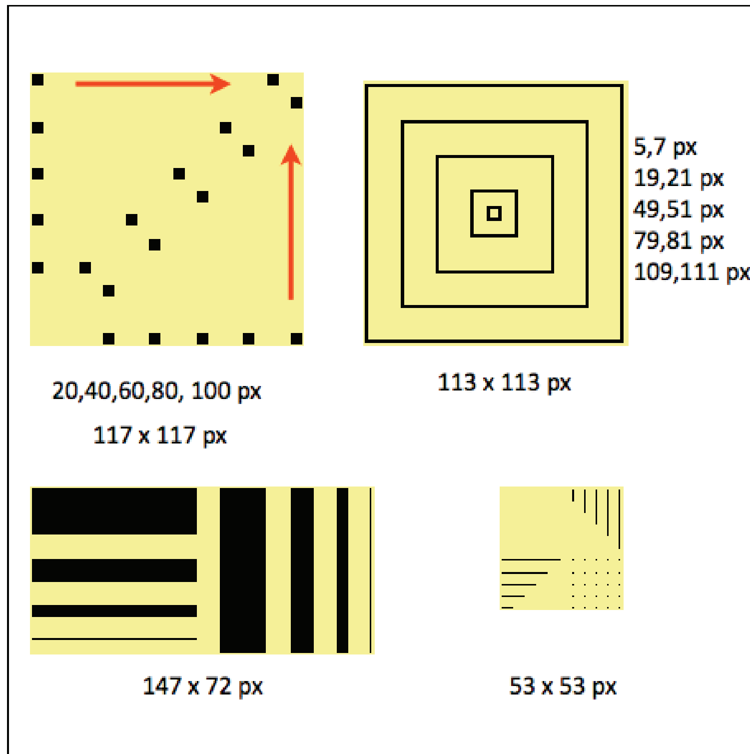

Figure 1: A set of test patterns for measuring the precision of our automated STM lithography. They test precision of jumps up to 100px, widths for narrow lines and spots and edge precision of multimode patterns.

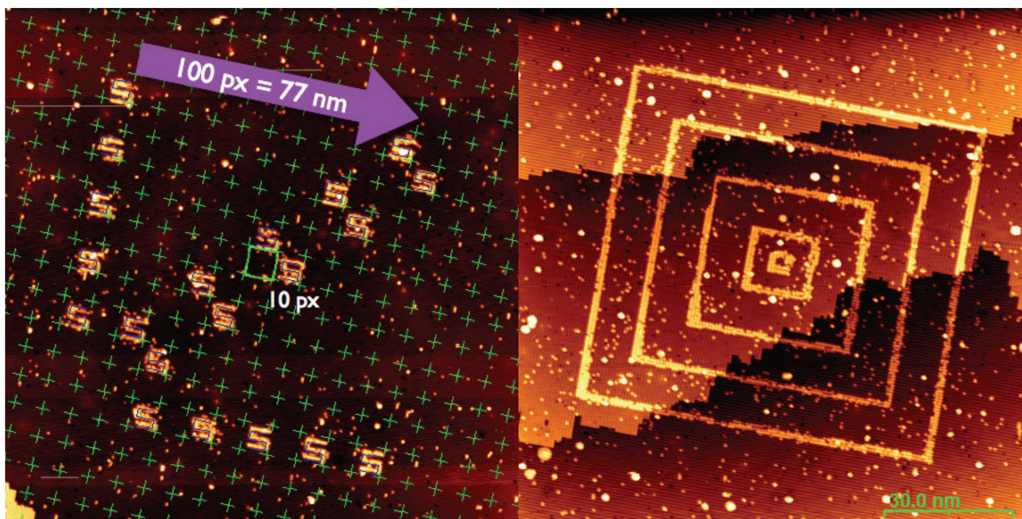

Figure 2: Example outputs of some of the test patterns shown in Fig.1, using real-time correction for piezo creep effects. At left, serpentines have been written up to 100 px apart with a maximum error of 1 px; At right, 10 rectangles have been drawn in 5 pairs, each pair making a 2-px-wide rectangle.