Nanometer precise overlay for sub-20nm thermal scanning probe lithography

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Thermal Scanning Probe Lithography[1] (tSPL) utilises a heated AFM tip to locally evaporate a polymer layer (see figure 1a). Nanometer precise 3D profiles can be formed[2] in the polymer layer (see figure 1b). tSPL offers a resolution and linear scan speed that is competitive[3] with the current state of the art maskless technique, Gaussian electron beam lithography. To utilise this lithographic capability a pattern transfer technique has been developed[4] and applied to the transfer of 18.3nm half pitch lines from the polymer layer into silicon[5]. Recently 13.9nm half pitch patterns were transferred into the commercial hard mask layer HM8006 (see figure 1c). To exploit these high resolution capabilities in the fabrication of devices nanometer precise overlay is required.

tSPL has a pair of unique capabilities for meeting this overlay challenge. Firstly it can read topography with sub-nanometer sensitivity and secondly reading the surface does not lead to resist exposure. Here we will demonstrate that the resist topography is not shifted with respect to the buried topography for sub-micron sized buried features. Further we will show that for reasonable sub-surface feature geometries the position of these features can be obtained from the resist profile with sub nanometer error. We will also outline the modifications we made to our home made tSPL system to achieve a 1.1nm 1sigma tool accuracy. Finally we will present recent work using our overlay capabilities to write electrical contacts to an InAs nanowire (see figure 1d).

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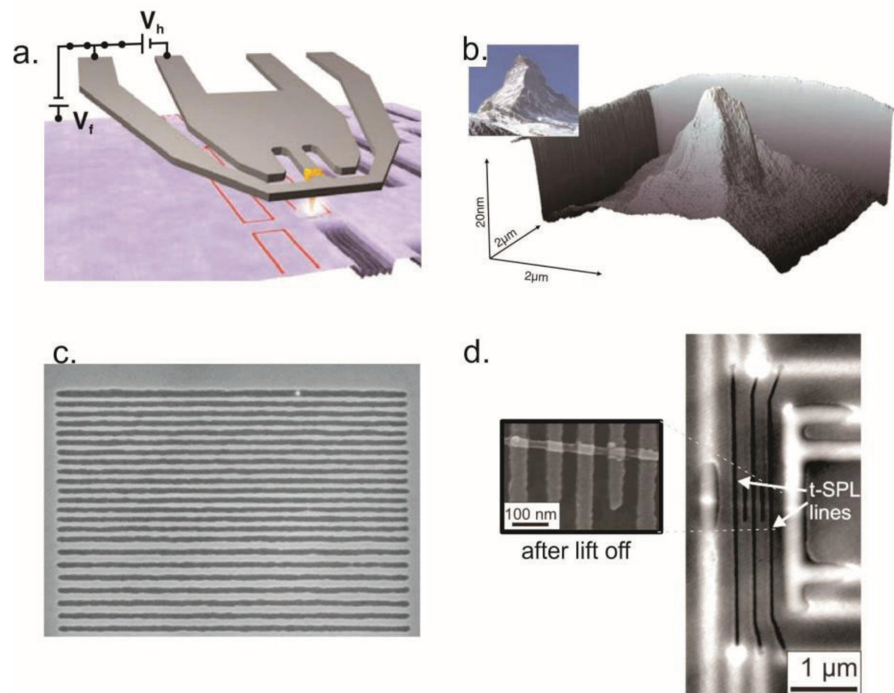

Figure 1 Introduction to thermal Scanning Probe Lithography. (a) Schematic of the writing process used in tSPL. The tip is heated by applying the voltage V_h this, in conjuction with the capacitive force due to V_f, leads to the removal of the polymer by the cantilever tip (figure reproduced from ref. 1) (b) A tSPL topography image of the Matterhorn (see inset) written into the substrate using the tSPL process (figure reproduced from ref. 1) (c) SEM image of parallel lines transferred into 30nm deep HM8006 hard mask layer. The lines were written using tSPL. The upper part of the field is written at a half pitch of 13.9nm while the lower part is written at 18.6nm. (d) Example of overlay of electrodes onto a 30nm diameter InAs nanowire. The image shows the measured topography following tSPL patterning. The dark lines show features written by the tSPL tool to a depth of 9nm. The inset shows an SEM image of the electrodes following pattern transfer and liftoff (reproduced from ref. 5).