Low DC-Bias Silicon Nitride Anisotropic Etching

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Silicon nitride is usually utilized as a dielectric layer between two metal layers. However, it is hard to pattern silicon nitride by common dry etching methods, which could result in short-circuit between the two metal layers, especially when silicon nitride is very thin. This is because high DC-bias voltage will sputter out those metal atoms everywhere (Figure 1). Wet etching of silicon nitride has no such problems but it is isotropic. This paper for the first time presents a research on low DC-bias silicon nitride anisotropic etching technology. Our etching results indicate that our new etching recipe (with DC-bias 34V and etching rate 40nm/min (Figure 2)) could not only eliminate short-circuit significantly but also achieve vertical etching sidewalls.

To achieve low DC-bias and anisotropic etching, we studied the effects of four factors on DC-bias and etching profile: reactive ion etch (RIE) power, ICP Power, pressure in the etching chamber, and the carbon-to-fluorine ratio (C/F). In the experiments, the silicon nitride film was deposited using PECVD and a Cr film patterned using photolithography, e-beam evaporation and lift-off was used as an etching mask. The machine used for etching was *Oxford Plasmalab System 100*. The etching gas used here were SF_6, C_4F_8, and O_2. To reduce physical bombardment, we did not use Argon in our recipe.

As shown in Figure 3(a), when the RIE power increases, DC-bias will increase monotonically. There is an activation RIE power below which the DC-bias will keep zero. However, at this activation point DC-bias is not stable. As ICP power increasing, etching rate will increase, and DC-bias will first increase then decrease (Figure 3(b)). The turning point will increase when pressure increases. DC-bias will first increase (Figure 3(c)) then decrease with increasing pressure. However, at high pressure, the etching rate is very slow. When total flow rate is constant and pressure is low, DC-bias will decrease if C/F ratio increases (Figure 3(d)). We also found that when DC-bias is lower, etching will be more isotropic (Figure 4(a)). That is due to less physical bombardment of ions to remove the passivation layer and enhance the chemical etching rate at the bottom. Figure 4(b) shows “beak-like” structures at the top edge of silicon nitride. That is because activation period lasts several seconds to allow DC-bias to increase from zero to certain stable values. So at first it is isotropic chemical etching and then there is more physical etching. Eventually, we achieved the etching recipe (*SF_6: 8 sccm, C_4F_8: 22 sccm, RIE power: 6W, ICP power: 300W, Pressure: 5 mtorr*), which can etch thin (*e.g.* 50nm) silicon nitride layer sandwiched between two 30nm chromium layers anisotropically without causing short-circuit between two metal layers.

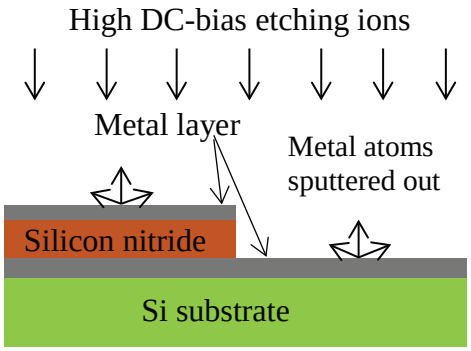

Figure 1: High DC-bias etching: metal atoms sputtered out, leading to short-circuit between two metal layers.

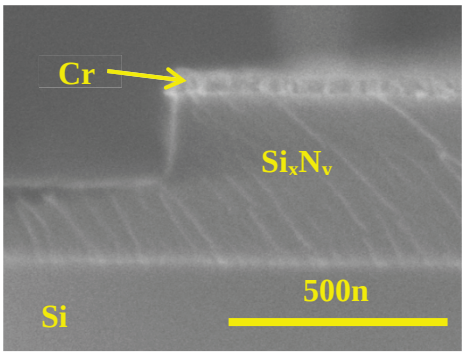

Figure 2: low DC-bias silicon nitride anisotropic etching: DC-bias 34V, etching rate 40nm/min.

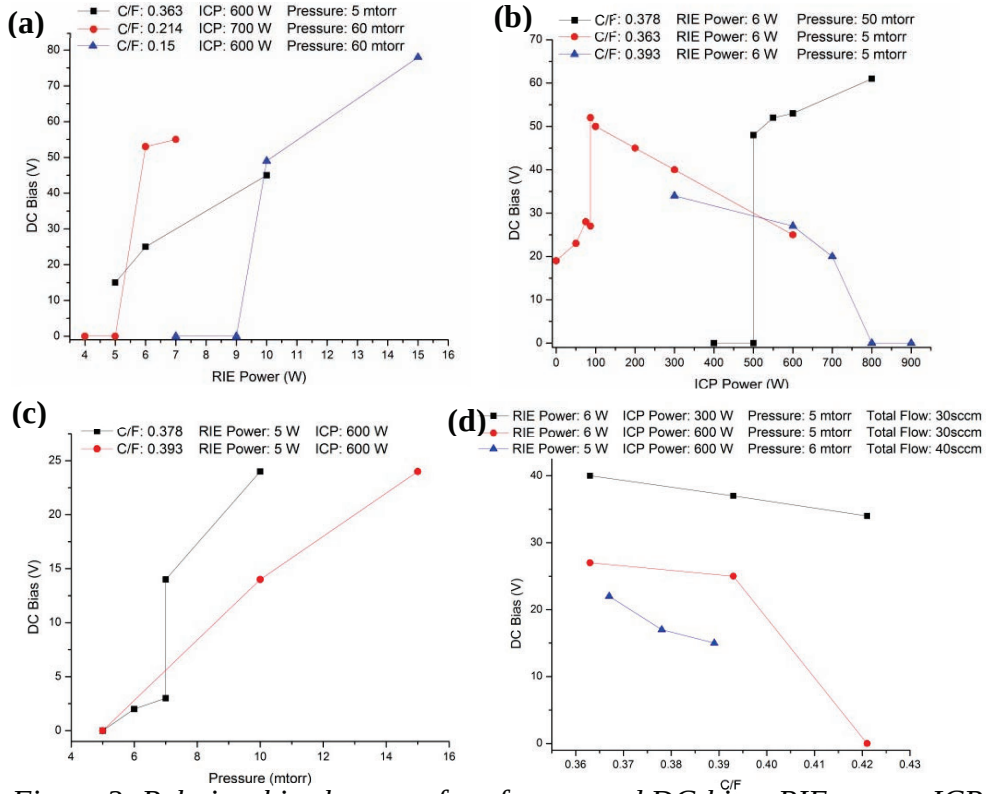

Figure 3: Relationships between four factors and DC-bias: RIE power, ICP Power, pressure in etching chamber and C/F ratio.

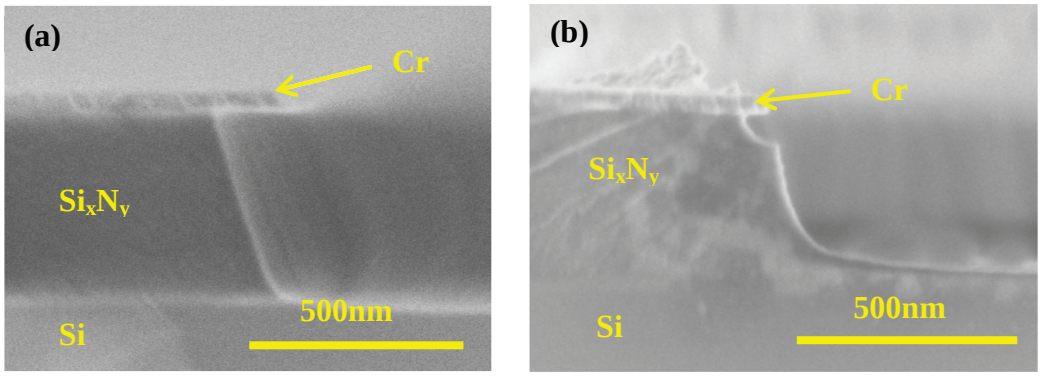

Figure 4: (a) Lower DC-bias, more isotropic. (b) "Beak-like" structure due to DC-bias increasing in activation period.