Stencil lithography for damage free fabrication of short channel photo conductive devices in graphene

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Stencil lithography (SL) is a high resolution shadow mask technique that allows the patterning of structures and devices such as metallic nano-dots, nanowires and NEMS. Compared to other techniques such as EBL, NIL and DUV/EUV lithography, SL has important advantages of not requiring any resists or light/e-beam exposure to avoid potential damage on the lattice structures of graphene. Based on this motivation, this work attempts to apply SL for the fabrication of interdigitated electrodes as a comb shape on graphene with the line dimension of 200 nm. The overall comb size is 60 µm x 50 µm. The whole device functions work as a photo-conductive sensor in a broad wavelength. The main challenge is to fabricate the stencils in SiNx membranes with the comb pattern. Especially when the comb size increases, the mechanical strength might be not strong enough to support the whole comb. The solution to this problem is to develop a mix-and-match process by combining the SL with optical lithography for the fabrication of graphene based nanodevices with interdigitated electrodes. In this case, the stencil has the pattern of 200 nm lines, and the common leads are completed by optical lithography, as schematically shown in figure 1.

A reactive ion etch (RIE) on SiNx in fluorine based plasma was then carried out using the patterned PMMA as an etch mask. (Figure 2) RIE tests were conducted to achieve the desired selectivity of SiNx over PMMA. (Figure 3) JEOL6300 FS and RIE were carried out to replicate 200 nm lines in in-house made SiNx membranes with the thickness of 100 nm – 300 nm. A deposition of metallic film such as Pd/Au directly on the SO_2 forms a 200 nm lines grating.(Figure 4) The common electrodes are then fabricated by optical lithography using the alignment marks fabricated on the stencils.

By summary, in this paper, we propose to use SL combined with optical lithography to fabricate 200 nm interdigitated electrodes on graphene for short channel devices in ballistic transport regime at room temperature thanks to the high mobility of the carriers. The success of this process will allow us to investigate the quantum transport of graphene at room temperature for novel nanodevices.

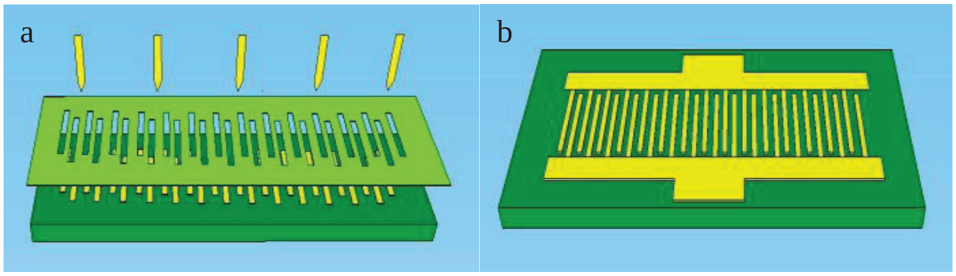

Figure1. Stencil lithography for interdigitated electrodes. (a) SL for the 200 nm Au-lines; (b) Electrodes by optical lithography.

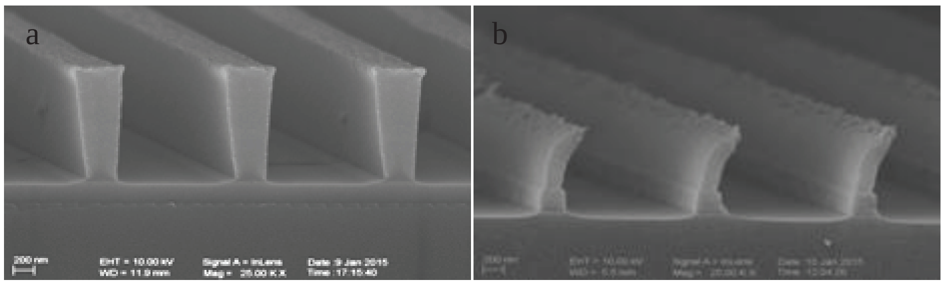

Figure 2.SEM image of interdigitated electrode pattern.(a) The sectional view with 1500nm PMMA on the 350nm SiN, width of 200 nm, 1500 nm period ; (b) the SEM image of RIE etch 1500 nm PMMA,350 nm SiN(CHF_3,50sccm,O_2, 5 sccm,5Pa,100W,15min), width of 200 nm, 1500 nm period .

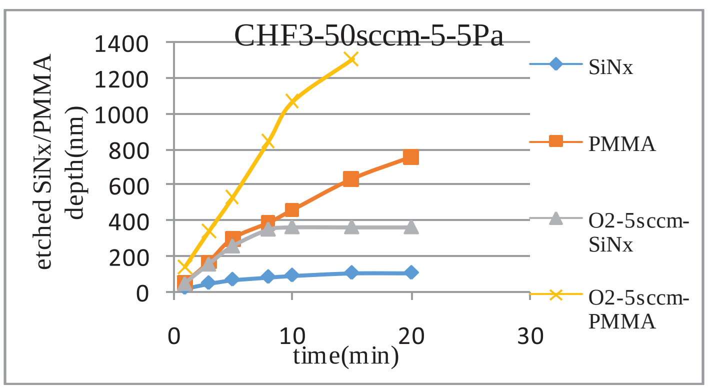

Figure 3. the desired selectivity of SiNx over PMMA

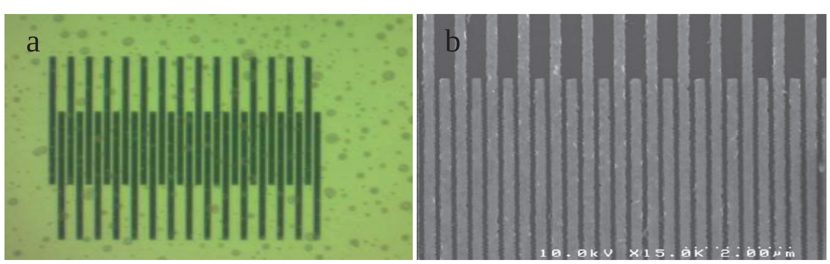

Figure 4. Optical microscope image or SEM of interdigitated electrode pattern.(a) The top side with stencil in the 100 nm SiNx membrane, width of 200 nm, 1.5um period.;(b) The top side with gold interdigitated electrodes on the 300 nm SO_2, width of 200 nm, 1.5um period.