Effects of thermal treatment on the transfer characteristics of sub-100 nm SnS_2 thin-film transistor arrays

Jeongsu Lee[1], Gunwoo Lee[1], Onejae Sul[2], Seung-Beck Lee[1,2,3]
[1]Department of Nanoscale Semiconductor Engineering, [2]Institute of Nano Science and Technology, [3]Department of Electronic Engineering, Hanyang University, 133-791, Seoul, Korea
sbl22@hanyang.ac.kr

Recently, transition metal dichalcogenide (TMD) thin-films such as, MoS_2, WS_2, and phosphorene have received much attention for their semiconducting properties at monolayer thicknesses[1]. Of these TMD materials, SnS_2 has a relatively high bandgap[2] of ~2.3 eV, which makes it fundamentally more applicable to thin-film transistors (due to lower leakage currents) and other novel nanoscale devices. However, there remain many device fabrication issues, such as nanoscale patterning, and metal contact, that need to be overcome for actual application.

Here, we demonstrate the fabrication of a sub100 nm SnS_2 thin-film transistor (TFT) array and also investigate the effects of thermal treatment on its transfer characteristics. We used a p^{++} Si/SiO_2 (90 nm) substrate as the back-gate structure. As shown in Figure 1(a), mechanical exfoliation was used to transfer 5 nm thick SnS_2 to the substrate. Then, electron-beam lithography on negative resist was used to define a 5 x 5 array of strips 60 nm wide and 500 nm long. For pattern transfer, reactive ion etching using SF_6 (5 mTorr, 30 sccm, 100 W) was used. After resist removal, Cr/Au (5/80 nm) source/drain electrodes were deposited using thermal evaporation. Figure 1(b) shows an SEM image of the SnS_2 TFT array after metal contact deposition, with the inset showing a single device. The I_D-V_G transfer characteristics after thermal treatments are shown in Figure 2. It can be seen that, after a rapid thermal annealing (RTA) treatment at 300 ^oC for 5 minutes, the subthreshold swing (SS) had been improved by ~75% enhancing gate coupling and the leakage current was reduced by ~97%. However, we observe a reduced on current and a positive shift of the threshold voltage (V_T). We attribute the enhanced SS to reduction of charges at the SnS_2/SiO_2 interface and possible desorption of gaseous molecules from the exposed SnS_2 surface. The reduced on-state current may be due to increased defects in the SnS_2 crystal, which would also cause the increase in V_T, reducing carrier mobility. An additional annealing step was performed at 200 ℃ for 2 hours under 760 Torr Ar pressure and showed similar changes as that after RTA. Raman spectroscopy analysis showed that after annealing, SnO_2 peaks were increased indicating that

[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, *Nat. Nanotechnol*. **6**, 147 (2011)
[2] H. S. Song, S. L. Li, L. Gao, Y. Xu, K. Ueno, J. Tang, Y. B. Cheng, and K. Tsukagoshi, *Nanoscale* **5**, 9666 (2013)

the reduced on current may be from oxidation of Sn causing increased scattering and reduced mobility.

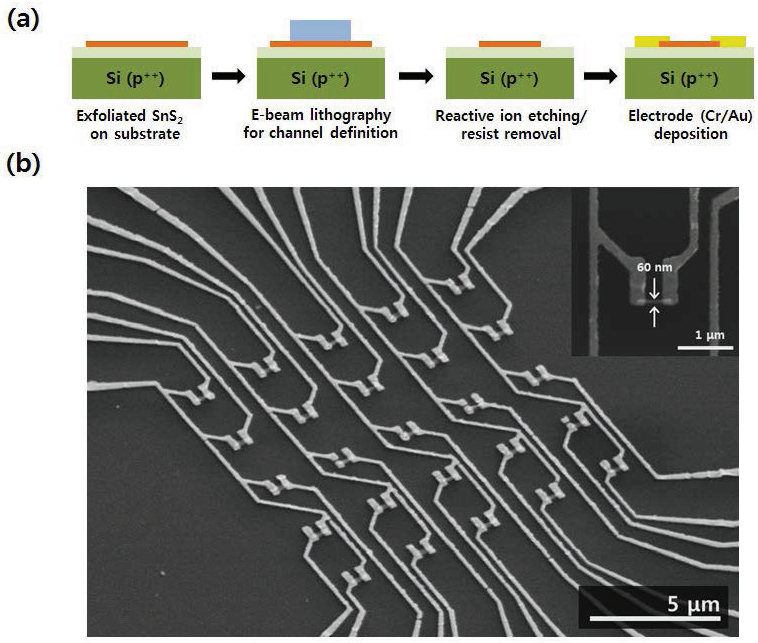

Figure 1: Fabrication of 5 x 5 SnS_2 TFT array. (a) Schematic diagram of the fabrication procedure. (b) Scanning electron microscopy (SEM) image of sub 100 nm SnS_2 TFT array. An image of a single SnS_2 TFT is shown in the inset

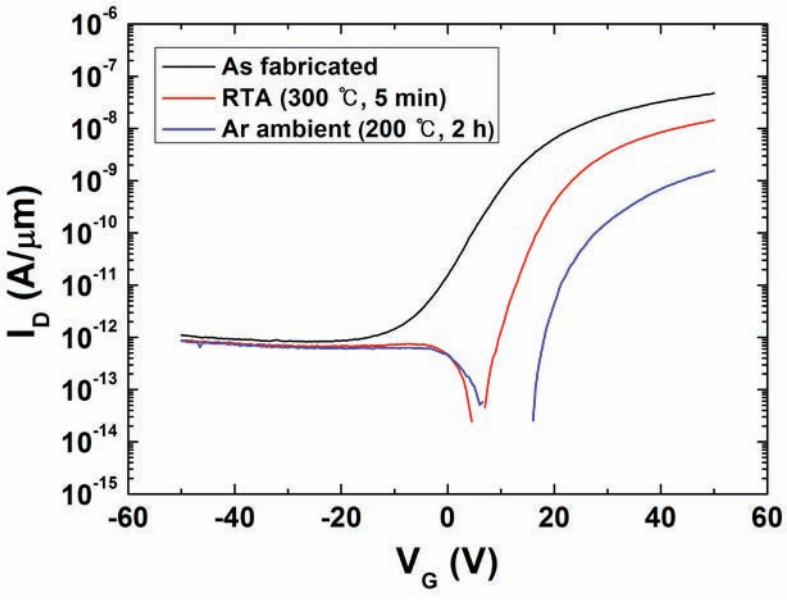

Figure 2: Electrical transport properties of a SnS_2 TFT: I_D-V_G curve of a SnS_2 TFT before and after thermal treatment. A drain bias of 1 V was applied, with gate bias ranging from -50 to 50 V.