Novel method for fabrication of sub-50nm multi-tier nanoimprint lithography template

P. Joseph and S.V. Sreenivasan

Department of Mechanical Engineering and NASCENT Engineering Research Center, The University of Texas at Austin
Email: praveenjoseph@utexas.edu

Nanoimprint lithography[1, 2] is a high throughput, low-cost lithographic technique that has demonstrated sub-10nm feature resolution and is widely accepted as one of the potential successors to optical lithography. However, challenges such as alignment and overlay need to be addressed before this technique can be used to pattern high density nanoelectronic circuits, especially on flexible substrates. Self-aligned multi-tier imprint lithography can eliminate alignment and overlay steps completely and has been demonstrated as an approach to fabricate micron-scale thin-film devices on flexible substrates and on glass.[3, 4] Applying the methodology to nano-scale patterning requires in turn, fabrication of multi-tier templates that may not be achievable using conventional optical lithography[4] or e-beam lithography[5] for the same challenges of nano-scale overlay and alignment.

In this work, we describe a novel fabrication process (figure 1) to make high resolution (sub-50nm) multi-tier nanoimprint templates, while eliminating the need for any alignment or overlay. The process involves a wafer-scale nanoimprint patterning step, followed by reactive ion etch (RIE) based pattern transfer into silicon dioxide, atomic layer deposition (ALD) of titanium nitride (TiN), and TiN spacer based second level etch to define the multi-tier template pattern. We have shown that our process is successful on resist pillars that can be transferred into telescoping features on silicon dioxide. We have also pushed resolution limits and demonstrated that our process works on high density grating resist features to form sub-50nm multi-tiered grating features on silicon dioxide (figures 2 & 3).

These templates are planned to be used for patterning high resolution devices on rigid and flexible substrates by nanoimprint lithography.

This work is supported primarily by the National Science Foundation under Cooperative Agreement No. EEC-1160494.

---

[1] B.D. Gates, *et al., Chem. Rev.* 2005, 105, 1171-1196.
[2] H.J. Levinson in *Proceedings of SPIE*, Vol. 8886, 888602, 2013.
[3] C.P. Taussig, P. Mei, H.J. Kim, *United States Patent US 7,202,179 B2*, Apr.10, 2007.
[4] E. Lausecker, *et al., Appl. Phys. Lett.* 96, 263501, 2010.
[5] S. Johnson, *et al., Microelectronic Engineering* 67-68 (2003), 221-228.

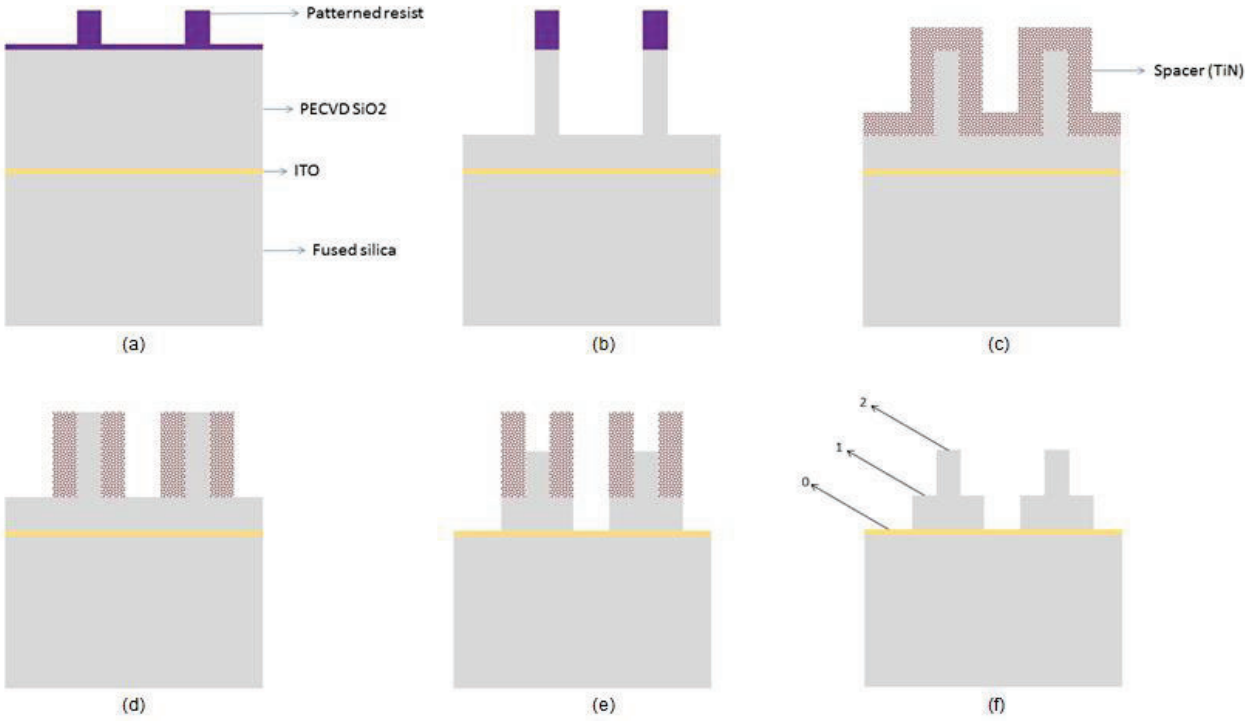

Figure. 1. Illustration of the multi-tiered template fabrication process. (a) Single tier patterns created using UV nanoimprint lithography, (b) Residual layer etching followed by first level etching of silicon dioxide, (c) removal of resist mask and atomic layer deposition of titanium nitride (TiN) on silicon dioxide (d) Etching of TiN to define side wall spacers (e) Second level silicon dioxide etching using TiN spacers as hard mask, (f) Removal of TiN hard mask to reveal multi-tiered SiO_2 features.

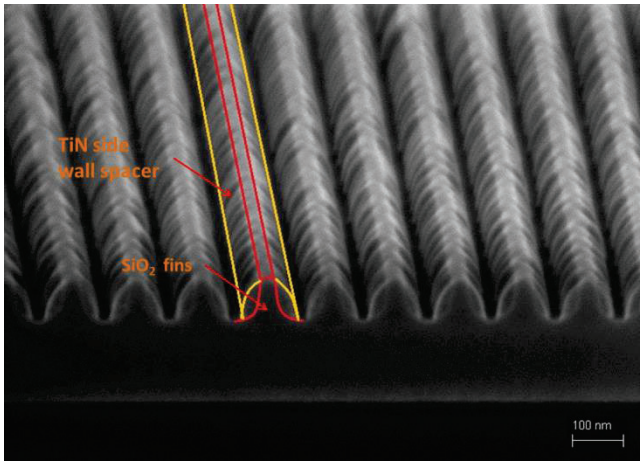

Figure 2. SEM Micrograph of etched silicon dioxide showing patterned side wall spacers. The scale bar is 100nm.

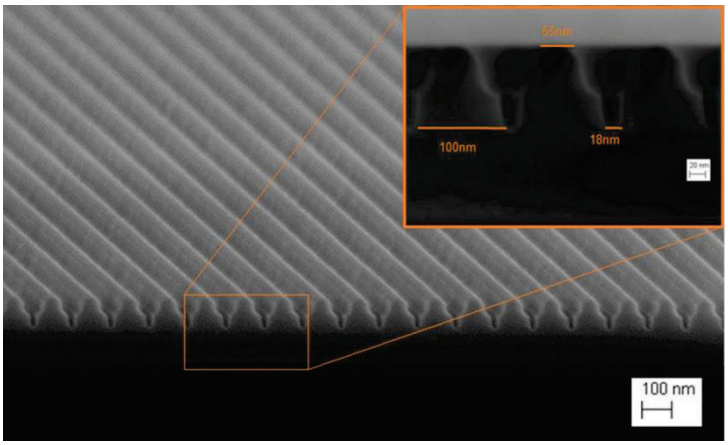

Figure 3. SEM Micrograph of sub-100nm multi-tier imprint template features on SiO_2 patterned using only one lithography step. The scale bar is 100nm.