Invited: Pattern-generation and pattern-transfer for sub-10nm devices

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The manufacturing of new sub-10nm electronic and optical devices requires the establishment of two fundamental technologies: lithography and pattern transfer. Herein, we show that novel future device concepts benefit from a closed-loop optimization between pattern-generation and pattern-transfer as opposed to serial optimization. Particularly this way, the demands of ever shrinking feature sizes, which include together line edge roughness, pattern alignment and process control can be fulfilled.

Today, high resolution lithographic techniques are typically linked with high capital investment in equipment. As a result, fast prototyping of novel devices is restricted. Here, we present a relatively low cost, fast prototyping lithography, Scanning Probe Lithography (SPL) [1] based on Fowler-Nordheim (FN) electron emission from a scanning proximal probe-tip [2]. This is combined with pattern transfer techniques, including the crucial contribution of cryogenic etching for pattern transfer [3]. The patterning tests are carried out in calixarene molecular glass resist 5 to 20 nm thick [4] by using a table–top SPL technology platform [5]. We have demonstrated the application of a step-and-repeat SPL method including optical as well as atomic force microscopy-based navigation and overlay-alignment. A mix-and-match approach is used to enhance throughput capabilities [6]. The closed-loop lithography scheme is applied to sequentially write positive and negative tone features. Due to the integrated unique combination of read–write SPL-cycling, each lithographic feature is aligned using AFM-methods with the highest positioning accuracy. In addition, each feature is AFM-inspected with the same tip after the writing. Routinely we can create a pattern in a step-by–step mode. Finally, we have demonstrated the patterning over larger areas and the practical applicability of the SPL processes for lithography down to 13-nm pitch patterns.

Pattern-transfer into silicon is a crucial technology in the modern manufacturing of integrated circuits (ICs) and microelectromechanical systems (MEMS) [7]. The process is in large part responsible for the continuous miniaturization of semiconductor devices, allowing the continuation of Moore's law, and for the shrinkage of MEMS devices to nano electromechanical systems (NEMS). The plasma based pattern transfer process is well established for moderate aspect ratios and linewidths down to 25nm and for HAR in the 50-100 nm regime. However, as feature sizes shrink, approaching 5nm regime for 'Beyond CMOS' devices, feature size and profile shapes must be controlled with tolerances approaching single nanometer dimensions [8, 9].

In this presentation, we will discuss silicon cryo-etching as an alternative approach to control feature profiles at the nanometer scale. We present pattern transfer of SPL lithography generated in sub-20nm thin calixarene nano-features and user simulations [10] of cryo-etching to understand the processes.

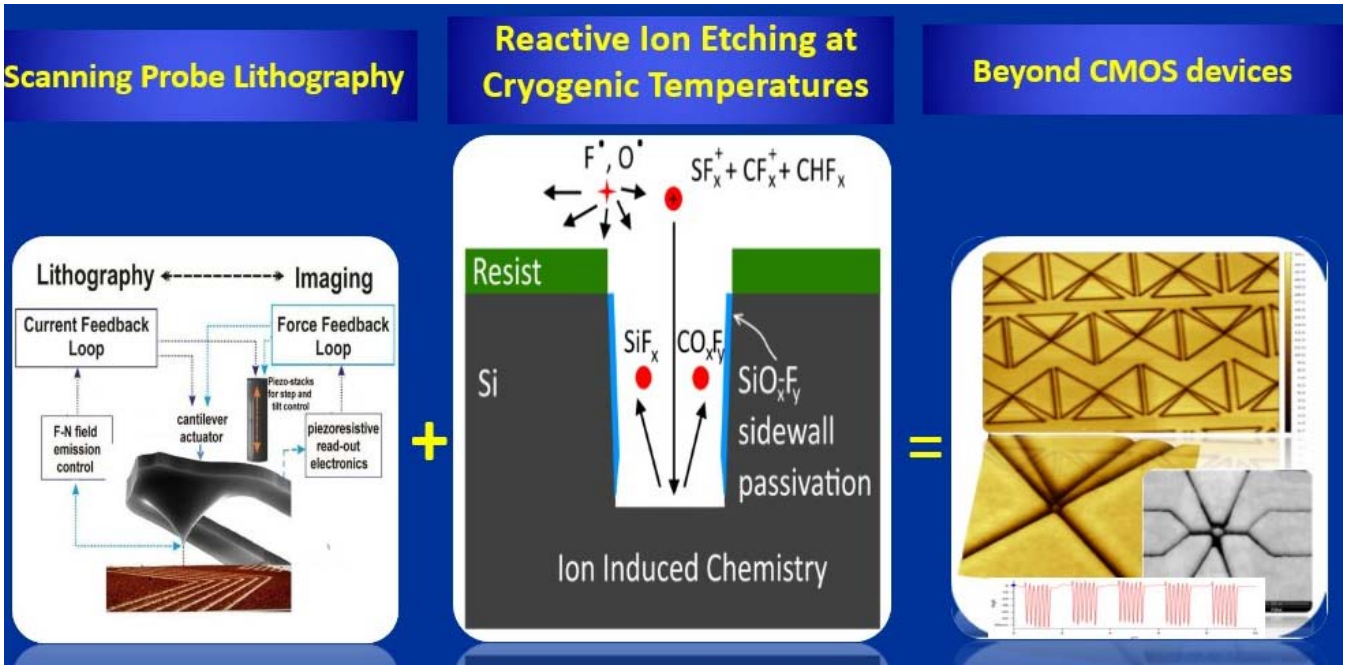

Fig.1: Combination of closed loop scanning probe lithography with cryogenic etching as a subsequent pattern transfer step employed for rapid prototyping of beyond CMOS device.

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