EUV Lithography for Advanced Nodes

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After more than two decades of fundamental research and development, Extreme Ultraviolet (EUV) lithography is slated to enter the IC manufacturing flow for critical levels in advanced nodes. The benefits of EUV Lithography are clear; higher resolution leading to better yield with fewer masks and processing steps [1]. This is particularly attractive for layers using complex multiple patterning schemes such as lithoetch-lithoetch-lithoetch (LELELE) or self-aligned multiple patterning (SAXP) on immersion 193nm lithography systems. Despite the clear advantage, there are many challenging problems that must be solved. Insertion of EUV lithography is being enabled by key improvements across many areas: mask infrastructure, mask manufacturing, mask pellicle, tool availability, source power, resist materials and computational lithography. This talk will focus on advances in the areas of resist materials and computational lithography.

While EUV resists are still relatively immature, they have improved over the past two years as EUV photons became more plentiful. Initial resists suffered from micro-bridging, top loss, pattern collapse, large line edge roughness (LER), poor local critical dimension uniformity (LCDU) and resolution less than what the optical contrast would suggest. Tuning the quencher chemistry and concentration has enabled traditional chemically amplified resists to resolve smaller features. New metal containing resists have also been proposed to improve EUV photon absorption and thereby reduce the amount of stochastic variations and improve the LCDU. Since metal oxide resists are more etch resistant, they can also be made thinner to help mitigate pattern collapse. Recent publications have demonstrated 13nm half pitch printing with standard chemically amplified EUV resists [2] and with metal oxide resists [3].

To achieve the ultimate resolution of EUV coupled with design flexibility, source and mask optimization (SMO) must be applied. SMO is a widely applied resolution enhancement technique for low-k1 imaging that employs constraints or cost functions to generate co-optimized illuminators and mask shapes which enable the success of downstream mask processing and wafer imaging [4]. In EUV imaging, the stochastic variability and line edge roughness are process limiting factors which should be minimized by the source. The inclusion of ILS in the source mask optimization through cost functions or constraints is therefore critical to lowering the line edge roughness [5].

Sub-resolution assist features (SRAFs) are another technique for improving process window. Optimal assist feature placement enables concurrent and expanded process windows for semi-isolated and isolated features. The application of EUV assist features requires a modified approach due to the non-telecentricity of the EUV imaging system. Typical symmetric placement of assist features creates phase errors that contribute to Bossung tilts and best focus shifts of individual features [6]. EUV assist features for semi-isolated and isolated features requires asymmetric spacing to prevent the phase errors in the diffracted orders.

While advancements in resist are needed to meet final production requirements, ILS based computational metrics can be helpful in setting realistic boundaries for design printability during technology definition. By calculating the available ILS, the final technology solution will be a co-optimization of not just the source and mask, but of the resist as well.

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