"Sketch and Peel" Lithography

Yiqin Chen¹, Quan Xiang¹, Zhiqin Li¹, and Huigao Duan^{1*} 1 School of Physics and Electronics, Hunan University, Changsha, China * Email: duanhg@hnu.edu.cn

Reliable definition of artificial micro- and nano-scale structures by lithographic processes is essential in a variety of fields including electronics, nano-optics, and bio-science. Among the well-developed lithographic methods, electron-beam direct writing (EBDW) is most commonly used due to its capability of fabricating original patterns with high resolution and flexibility.[1] However, a typical EBDW process is extremely time-consuming for large-area patterning due to the point-by-point serial scanning manner. Additionally, the intrinsic scattering between electrons and the samples results in proximity effect that makes the definition of fine structures challenging.[2] These two issues have severely limited the broader applications of EBDW.

In this work, we propose an EBDW strategy, termed "Sketch and Peel" lithography (SPL), which could enhance the patterning efficiency up to hundreds of times higher and significantly mitigate the proximity effect compared to conventional EBDW process. The basic fabrication process flow of SPL is schematically shown in **Figure 1a** and demonstrated in **Figure 1b-1e**. Compared to conventional EBDW process, the key idea of SPL is that only the outline of the target structure is exposed and the central area is subsequently filled by selectively peeling off an evaporated metal layer outside and on the top of the outline. This SPL process has a similar step with existing "brushfire" lithography^[3,4] by using the advantage of outlines. However, the dry peeling process in SPL is much easier to implement in practice and promises high resolution and clean surface for real applications.

With the advantage of reduced exposure time, high-fidelity metallic micro- and nanostructures could be fabricated over large area using SPL strategy (**Figure 2a**). Particularly, with SPL process, metallic nanogaps down to 15 nm (**Figure 2b-2c**), which are challenging to achieve in the past due to the severe proximity effect, could be directly and reliably defined with much less time for potential optical and electronic applications. With significant enhanced throughput and mitigated proximity effect, the SPL process promises great extension of the capability of EBDW technology for faster patterning of high-quality metallic structures with nanometer precision.

- [1] J. K. Yang *et al.*, *J. Vac. Sci. Technol. B* 27, 2622-2627 (2009).
- [2] H. Duan *et al. J. Vac. Sci. Technol. B* 28 H11-H17 (2010).
- [3] T. A. Fulton, G. J. Dolan, Appl. Phys. Lett. 42, 752-754 (1983).
- [4] G. J. Dolan, T. A. Fulton, IEEE Electron Device Lett. 4, 178-180 (1983).

Figure 1. Basic fabrication process of "Sketch and Peel" lithography (SPL). (a) The three-dimensional schematic flow-charts to show the methodology of SPL process. (b-e) The series of four SEM images successively present the corresponding result of 1-μm ring HSQ templates, Au-coated HSQ templates, as-stripped gold disk array, and pure gold disk array with the removal of HSQ rings. The upper-right insets clearly show the corresponding enlarged electron micrographs of single structures in the array. All scale bars are 2 μm.

Figure 2. Gold structures fabricated by SPL process. (a) Scanning electron micrograph of a 3-µm gold triangle array with the pitch of 6 µm. Inset show the corresponding colorful photography of large-area gold triangle array $(5 \text{ mm} \times 5 \text{ mm})$. (b) Arrayed sunflower-like artificial molecules which have a uniform gap size of \sim 15 nm among the densely-packed parts. The central disk was 500 nm in diameter. (c) Zone-plate-like gold pattern with the maximum diameter of 15 μ m, in which all gaps were \sim 15 nm. Scale bars: (a) $3 \mu m$, (b) $1 \mu m$, (c) $2 \mu m$.