

# Toward high-performance nanoelectronics based on carbon nanotubes

Shu-Jen Han

*IBM T. J. Watson Research Center, Yorktown Heights, NY 10598*

*sjhan@us.ibm.com*

In the last four decades, we have witnessed a tremendous information technology revolution originated from the relentless scaling of Si complementary metal-oxide semiconductor devices. CMOS scaling provides ever-improved transistor performance, density, power and cost, and will continue to bring new applications and functions to our daily life. However, the conventional homogeneous scaling of silicon devices has become very difficult, firstly due to the unsatisfactory electrostatic control from the gate dielectric. In addition, as we look forward to the technology nodes with sub-10 nm channel length, non-Si based channel materials will be required to provide continuous carrier velocity enhancement when the conventional strained-Si techniques run out of steam.

Low-dimensional carbon materials are promising to replace silicon as the channel material for high-performance electronics near the end of silicon scaling roadmap, with their superb electrical properties, intrinsic ultrathin body, and nearly transparent contact with certain metals. In this talk, I will cover recent progress within IBM Research as well as the discussion that highlights most significant challenges from technology points of view.<sup>1,2,3,4,5</sup>

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<sup>2</sup> Q. Cao, S.-J Han, G. S Tulevski, Y. Zhu, D. D Lu, W. Haensch, "Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics," *Nature Nanotechnol*, 8, 180-186, 2013

<sup>3</sup> S.-J. Han, S. Oida, H. Park, J.B. Hannon, G.S. Tulevski, W. Haensch, "Carbon Nanotube Complementary Logic based on Erbium Contacts and Self-Assembled High Purity Solution Tubes," *IEDM*, 2013

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<sup>5</sup> Q. Cao, S.-J. Han, J. Tersoff, A. D. Franklin, Y. Zhu, Z. Zhang, G. S. Tulevski, J. Tang, W. Haensch, "End-bonded contacts for carbon nanotube transistors with low, size-independent resistance," *Science*, 350, 68-72, 2015