3D Hybrid Memristor/CMOS Circuits with 8 Monolithically Integrated Crossbar Layers

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3D hybrid memristor/CMOS circuits are feasible solutions to meet the ever-growing demand in capacity and functionality for memory, logic and neuromorphic applications[1]. In this paper, we demonstrated the monolithic integration of up to 8 memristor crossbars layers with foundry-made CMOS chip. The Pt/HfO2/TiN memristive devices were engineered to be electrically compatible with the CMOS circuits. Reliable switching performance of the memristive devices was achieved in the integrated chips with reset current down to sub-1μA level.

The integrated hybrid circuit adopted a CMOL-like architecture[2] (fig. 1a). Multilayer memristor arrays were fabricated direct on top of a foundry-built CMOS chip (fig. 1b-c). The basic principle is utilizing an area-distributed via array between CMOS and memristor crossbar layers for interconnection. Each memristive device in the stacked crossbar layers can be uniquely accessed from the four-dimensional address space. The layout of the stacked device layers was designed so that the same photomasks can be repeatedly used for every two layers. We used a UV-curable resist as the passivation and planarization layer (fig. 2b). The room temperature crosslinking process ensures its compatibility with the back end of line processing. Meanwhile, we created a V-shape profile for the vias (fig. 2) and the tapered sidewall greatly reduced the thickness of the metal required for interconnection.

Fig. 3 shows the optical and SEM images of the integrated chips with 2 to 8 layers of memristor crossbars (Figs. 3a, 3b). The details of the crossbar devices are shown in the magnified optical and SEM images (fig. 3c-e). A cross-sectional SEM image of the 8-layer crossbar stacked on the CMOS chip is shown in fig. 3f.

The geometry of the Pt/HfO_2/TiN memristor used for the integration is shown in fig. 4a. The devices were carefully engineered to comply with the designed upper limits for the operational voltage and current of the CMOS chip (6V and 150 μA, respectively). Especially, we found the switching current can be effectively tuned by varying the N_2 partial pressure during the reactive sputtering of TiN electrodes. As shown in fig. 4c-f, by increasing the N_2 partial pressure from 12.5% to 37.5%, the switching current dramatically reduced from 1mA level down to 1μA level. Consistent switching performance was observed inside the hybrid circuit with ultralow switching current down to 820 nA (fig. 4h). The low switching current is critical to reduce the power consumption of the hybrid system.

In conclusion, we demonstrated the monolithically 3D integration of hybrid memristor/CMOS circuit with up to 8 layers of crossbar devices with ultralow operational current. This work shows great promise of hybrid memristor/CMOS integrated circuits in the next generation memory and neuromorphic applications.

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[1] J. J. Yang *et al*, *Nat. Nanotechnol.* **8** 13–24 (2013)
2. D.B. Strukov and R.S. Williams, *PNAS*, **106** (48), 20155-20158 (2009)

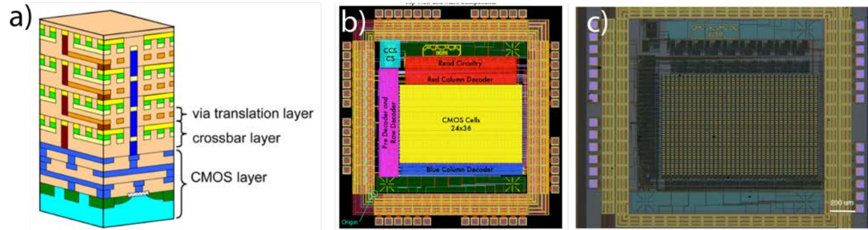

Figure 1: (a) schematic of CMOL-like 3D memristor/CMOS hybrid circuit[2]. (b) layout and (c) optical micrograph of the foundry-built CMOS chip for the integration.

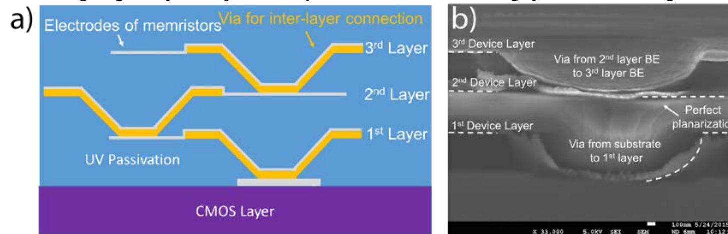

Figure 2: Interconnection between adjacent layers. (a) schematic of cascading V-shape vias for three device layers (b) cross-sectional SEM image of stacked V-shape vias.

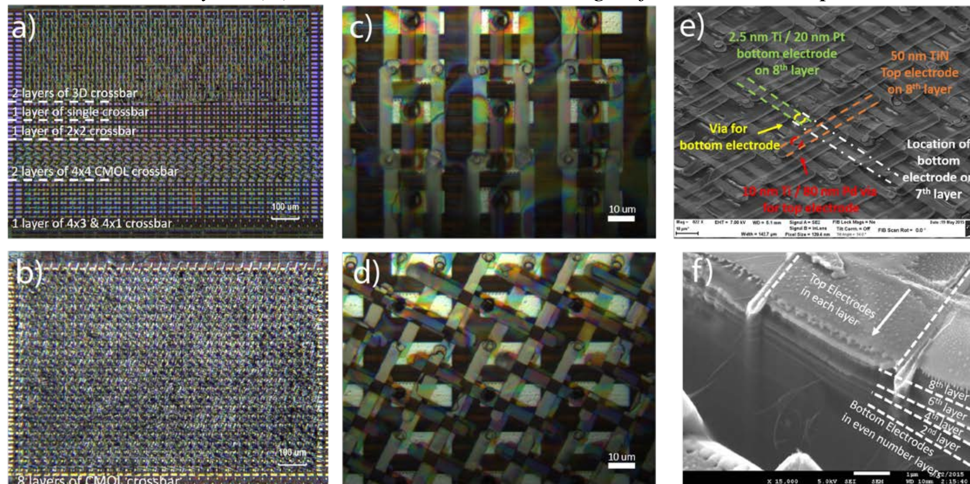

Figure 3: (a) optical image of a two-layer integrated chip with mix of device structures and (b) integrated chip with eight CMOL crossbar layers. (c,d) magnified images of the device area. (e) angled and (f) cross-sectional SEM images of 8-layer crossbar stacked on the CMOS chip.

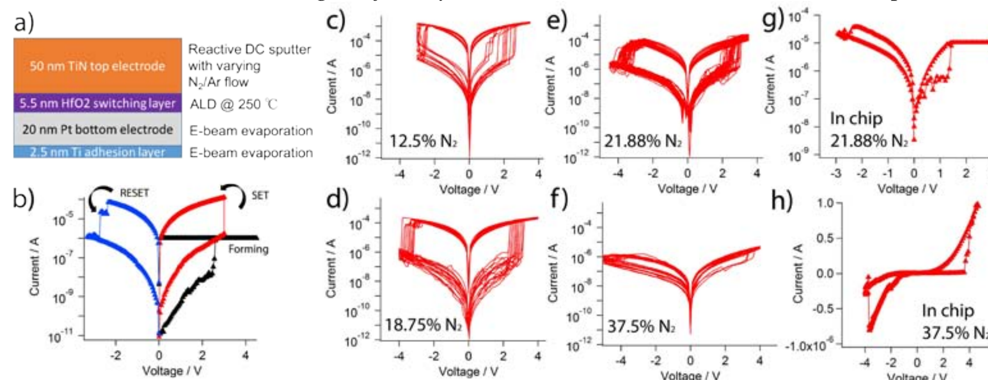

Figure 4: (a) schematic and (b) typical I-V characteristics of the Pt/HfO2/TiN device. (c-f) devices with different switching current tuned by varying the N_2 partial pressure during the reactive sputtering of TiN electrodes. (g) typical device behavior measured in the integrated chip. (h) ultralow switching current of 820 nA obtained in one of the integrated chip by using N-rich TiN electrodes.