Electron Spin Resonance Characterization of Damage and Recovery of Si/SiO_2 Interfaces from Electron Beam Lithography

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Confined electrons and donors in silicon are promising avenues for the realization of a quantum processor. Silicon has a naturally low percentage of nuclear spin isotopes along with a small spin orbit coupling and as such has demonstrated the longest electron spin coherence times in solid-state systems[1]. Quantum devices in silicon, such as single electron transistors[2], quantum dots[3], and quantum point contacts[4], all rely on nanoscale electrostatic gates that must be fabricated using electron beam lithography (EBL). However, high-energy electrons and photons from the EBL process create shallow traps and other defects at the Si/SiO_2 interface, inhibiting the control of electron populations. In fabricating these devices, it is essential to quantify the damage caused by EBL and to optimize processing parameters to reduce this damage.

Two common methods of reducing defects at the Si/SiO_2 interface are high temperature (~900C) and forming gas (~400C) anneals. We studied the effect of these anneals on the reduction of shallow traps (2-4meV in depth) created by EBL by fabricating two sets of large area (~1cm^2) MOSFETs and characterizing them with transport and electron spin resonance (ESR) measurements[5]. Both sets of MOSFETs were fabricated from the same commercially grown gate stack (30nm dry thermal oxide, 200nm amorphous silicon) and were implanted with arsenic (35keV, $5*10^{15}$ cm^{-2}) to dope the gate and form contacts. The MOSFETs were then etched in a fluorine-based plasma and were annealed at high temperature (900C, 1 hour, N_2 ambient). At this stage, the process was split and one set of MOSFETs was treated with a typical EBL exposure (10kV, 40μC cm^{-2}) while the other remained unexposed. The EBL exposed sample was then re-annealed at high temperature. Both samples then had aluminum contacts thermally deposited and received a forming gas anneal (25min, 435C).

Our transport data show that these anneals recover the EBL exposed low temperature (4.2K) peak mobility to 85% of the unexposed sample's peak mobility of 8,100 cm^2 V^{-1} s^{-1}. Additionally, our ESR data indicate that these anneals completely reduce the density of shallow traps between 2-4 meV of the EBL exposed sample to the same density as the unexposed sample ($2*10^{10}$ cm^{-2} meV^{-1}). In conclusion, we quantitatively demonstrate the efficacy of high temperature and forming gas anneals on reducing shallow traps formed at the Si/SiO_2 interface by EBL.

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