Imaging semiconductor patterns at N10 logic node with a high-throughput multi-beam SEM

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The continuous shrink of semiconductor patterns imposes many challenges on the fabrication of semiconductor devices, not only on the patterning process itself but also on the inspection of the patterns. The required resolution is becoming increasingly difficult to achieve with current optical inspection techniques. SEM-based inspection technologies can resolve the relevant patterns and defects, but have not been able to achieve the throughput requirements for screening large areas yet. This barrier has recently been overcome in 2014 with the introduction of multi-beam scanning electron microscopes [1].

The details of the setup of the multi-beam electron microscope have been described in detail elsewhere [1]. We describe the basic principle of operation in Figure 1: Multiple primary beams (depicted blue in the left image) are scanned in a single column in parallel over a sample (right image); one detector per secondary electron beam (green in the left image) enables parallel detection of all beams, thus circumventing the detector bandwidth limitation. The distribution of the current over a large volume inside the column enables maintaining high resolution at high total current.

In this paper, we apply the multi-beam SEM to the inspection of patterns on a semiconductor wafer suited for process window qualification at the N10 logic node. We will demonstrate that the multi-beam SEM is able to image the relevant patterns at this technology node, track their variations as the focus and dose conditions of the lithography scanner are varied, and find defects which will limit the process window for the lithography application. Example images taken with the multi-beam SEM can be seen in Figure 2.

[1] Eberle, A. L. et al., J. Microsc. **259**, p.114 (2015) [doi:10.1111/jmi.12224]

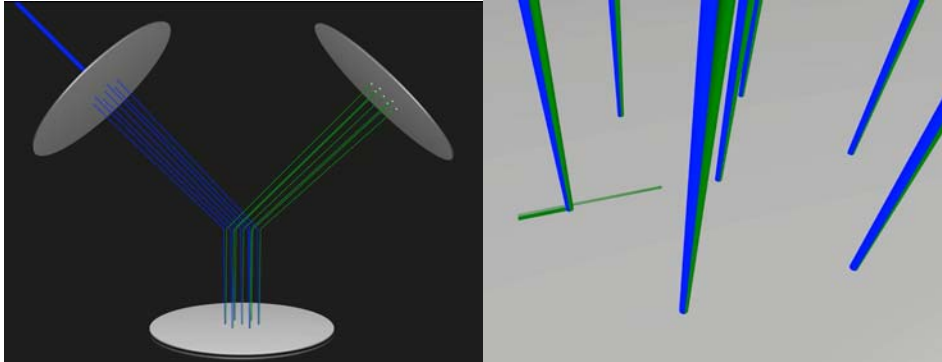

Figure 1: Left: Schematics of the multi-beam electron microscope. Right: detail of the parallel scanning process. For simplicity, 7 beams are shown only.

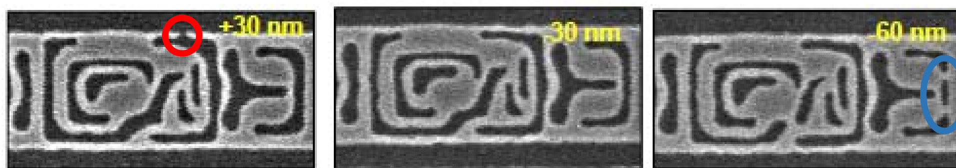

Figure 2: Images of a semiconductor wafer pattern at the N10 logic node, imaged with the multi-beam SEM. Nominal line width in these patterns is below 25nm. The center image shows the pattern as printed at the nominal best focus condition of the lithography scanner (-30nm), left and right image show the pattern as printed at defocus conditions of the lithography scanner. In the left image, one clearly sees a bridging type defect formed at the top of the image (red circle); in the right image one clearly sees the rightmost feature breaking apart (blue circle).