Overlay improvement in nanoimprint lithography for 1x-nm patterning

K. Fukuhara, M. Suzuki, M. Mitsuyasu, T. Komukai, M. Hatano, T. Kono, T. Nakasugi
Center for semiconductor research and development, Semiconductor and storage products company, Toshiba Corporation, Yokohama, Kanagawa 2358522, Japan
kazuya2.sato@toshiba.co.jp

Y. Lim, W. Jung
SK Hynix Japan Inc., Tokyo 1056023, Japan

Nanoimprint lithography (NIL) is becoming a promising technique for fine-patterning with lower cost than other lithography technique. High overlay accuracy is one of the big challenges in NIL. Using die-by-die alignment with moiré fringe detection, NIL alignment measurement accuracy below 1nm and overlay accuracy below 10nm has been reported. On the other hand, requirement for overlay in 2020 based on ITRS 2013 roadmap is as small as 3.9nm for flash and 3.1nm for DRAM. In order to qualify the overlay accuracy requirement from the semiconductor industry, a lot of technology enhancements, such as improvement of overlay control accuracy for NIL-tool, image placement accuracy improvement for NIL templates, mix and match technique of NIL and other lithography tool such as immersion exposure tool, are needed.

In this paper we describe evaluation of NIL overlay performance using the up-to-date NIL tool, and discuss potentials of NIL overlay in the future. Alignment accuracy, precision, and overlay correction performance of NIL tools, overlay error originated from master/replica template, NIL-to-NIL and NIL-to-immersion distortion matching performance, and overlay error structure analysis (intrashot, intrawafer, wafer-to-wafer, etc.) are discussed. Relation of overlay accuracy and throughput is also discussed. From these analysis based on NIL overlay data, we discuss possibility of NIL overlay evolution to realize adaptation to mass production for 1x-nm device.