Area-selective atomic layer deposition using e-beam and photosensitive masking layers

R.H.J. Vervuurt [a], *A. Sharma* [a], *Y. Jiao*[a] *W.M.M. Kessels* [a] *& A.A. Bol* [a]

[a] Eindhoven University of Technology, Eindhoven, 5600 MB, The Netherlands
e-mail: r.h.j.vervuurt@tue.nl

In conventional patterning processes a material is deposited first, then patterned, and subsequently the undesired parts are removed by etching. This top-down approach requires many processing steps which are expensive and time consuming. Furthermore, top-down processing is challenging when the materials are difficult to dry-etch such as Pd, Pt or Cu. One also risks damaging the underlaying layers, which is especially problematic for the up-and-coming 2D materials, for example graphene and 2D-MoS_2. To overcome the above mentioned issues area-selective processing techniques are gaining increasing attention. In area-selective processing the material is only deposited where required, avoiding the need of subsequent etch steps.

Area-Selective Atomic Layer Deposition (AS-ALD) makes it possible to selectively deposit thin films with excellent uniformity and conformality[1]. AS-ALD can be achieved by various means: 1) by area-deactivation, for example using self-assembled monolayers (SAMs) or thermally stable polymer films that block ALD growth or 2) by area-activation, for example using seed-layers that initiate ALD growth.

In this contribution AS-ALD of Pt using temperature stable polymer films that block Pt ALD growth is discussed. The resists used can be patterned using conventional photo and e-beam lithography, making implementation relatively straightforward. Pt is deposited on the patterned substrates using $MeCpPtMe_3$ as the precursor and O_2 as the reactant gas at 300°C. The optical micrograph in Figure 1, shows AS-ALD of Pt using PMMA and Polyimide. The process shows excellent selectivity. Pt is deposited on SiO_2, while no deposition occurs on the polyimide or PMMA. The PMMA patterns are however always 10µm smaller than intended. This is because the ALD deposition temperature lies well above the PMMA glass transition temperature, resulting in the reflowing of the resist, limiting the minimum feature size to about 20µm. Using polyimide, the Pt features created match the pattern sizes in the resist layer, the higher temperature stability (>375°C) preventing the reflowing of the polyimide (Figure 2). The minimum feature size obtained was 3.5µm, limited by the polyimide thickness and lithography tool used. The developed AS-ALD process is subsequently used to deposit Pt contacts on graphene by ALD (Figure 3). It will be discussed that the results can also apply to other materials as long as the ALD chemistry is unreactive towards the resist surface.

[1] A.J.M. Mackus, A.A. Bol & W.M.M. Kessels, *Nanoscale*, 2014, **6**, 10941

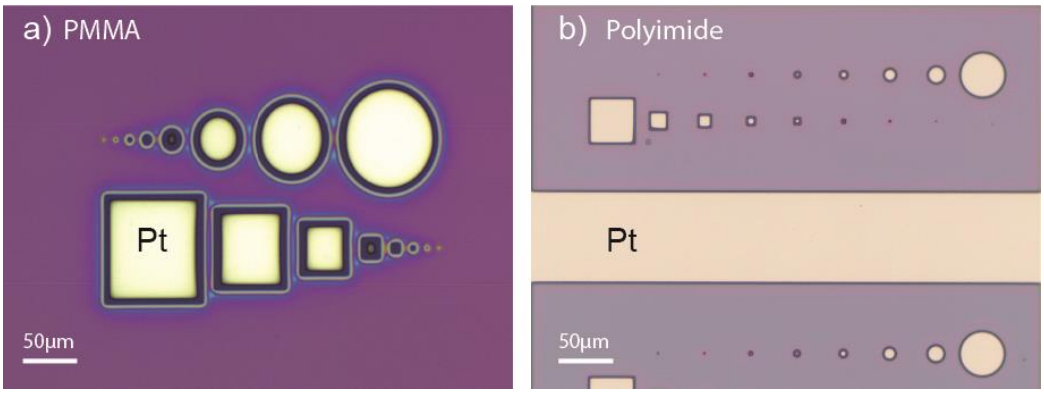

Figure 1: Optical micrograph showing the AS-ALD of Pt using a) PMMA and b) Polyimide. The colour change towards the feature edges for the PMMA pattern indicates a reduction of thickness as a result of the reflowing of the resist during the ALD process

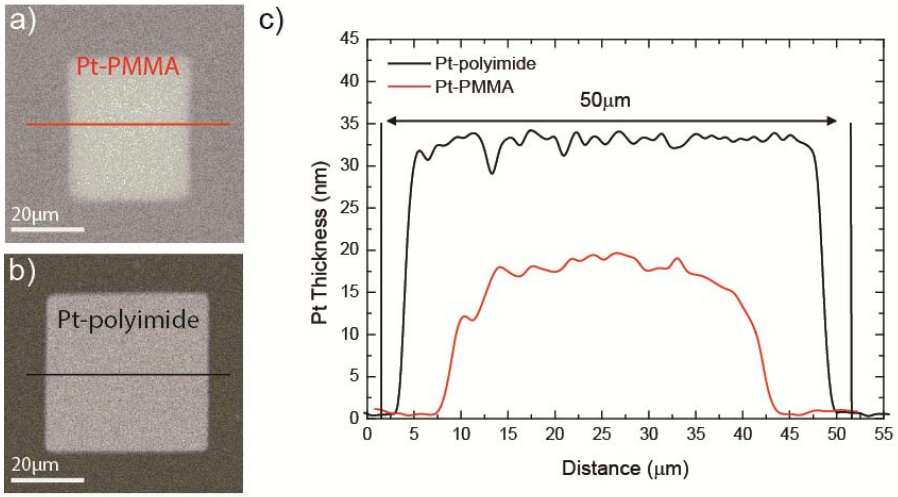

Figure 2: SEM micrograph of a) PMMA and b) polyimide created feature, the intended feature size was 50µm. The thickness of the Pt feature is show in c) determined from an EDX line scan. The position of the EDX scan is indicated by the red and black line in a) and b)

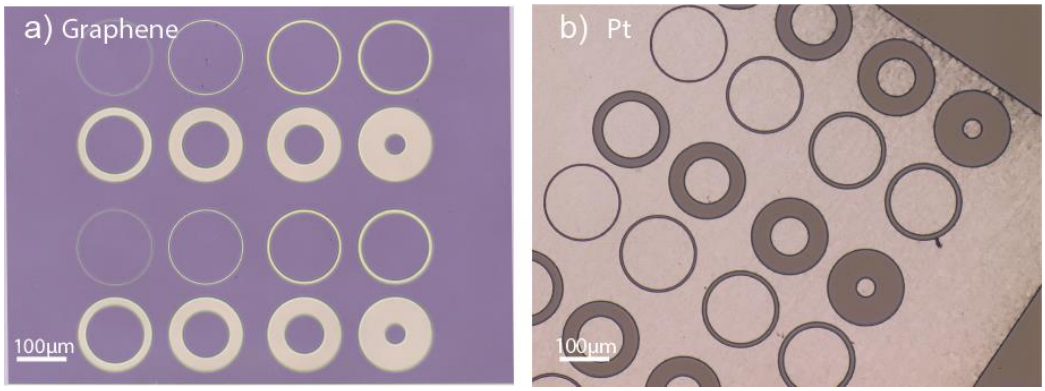

Figure 3: Optical micrograph showing the polyimide patterns on graphene a) after development and after 1000 cycles of Pt ALD.