

# Double-Gate Organic Micro-Electro-Mechanical Relay for Ultralow-Power Flexible Large-Area Electronics

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Organic thin film transistors (OTFTs) have been researched over the past decades to enable flexible large-area electronics [1]. Due to the organic materials (e.g., conjugated polymers and small-molecule materials) being employed as the active semiconductor layer however, OTFTs developed to date are subject to the following limitations: Firstly, relatively low field-effect carrier mobility of the active layer material (well below  $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ) requires a rather large supply voltage (typically  $> 10 \text{ V}$ ) for a reasonable on/off current ratio ( $> 10^5$ ); Secondly, relatively poor semiconductor/dielectric interface induces fairly large off-state leakage current ( $I_{\text{OFF}}$ ) [2]. Large  $I_{\text{OFF}}$ , coupled with such a large  $V_{\text{DD}}$ , would lead to large amounts of static and dynamic power consumption. To overcome the limitations and hence enable ultralow-power flexible large-area electronics, we propose a seemingly-different organic micro-electro-mechanical (MEM) relay as a potential alternative to conventional OTFTs since its unique switching characteristics such as zero  $I_{\text{OFF}}$  and abrupt on/off switching can provide for zero static power consumption and potentially very-low dynamic power consumption.

**Fig. 1** shows an isometric view, cross-sectional views, scanning electron micrographs (SEMs), and design parameters of a polymeric MEM relay of this work. The relay is an eight-terminal device, which has two gate electrodes (under the movable structure), two bodies, and two pairs of source/drain (S/D). The operating principle is the same as that for the relay designs in [3-4]: Briefly, the voltage applied between the gates and bodies ( $V_{\text{GB}}$ ) determines the on- or off-states of the relay. When  $V_{\text{GB}} \geq V_{\text{PI}}$  (pull-in voltage), the relay turns on, and current flows between S/D. When  $V_{\text{GB}} < V_{\text{RL}}$  (release voltage), the relay turns off. **Fig. 2(a)** shows near-zero  $I_{\text{OFF}}$  ( $\sim 10 \text{ fA}$ ), abrupt on/off switching, relatively high  $I_{\text{ON}}/I_{\text{OFF}}$  ratio ( $\sim 10^7$ ), and  $V_{\text{PI}}$  and  $V_{\text{RL}}$  that are tunable with the body bias. **Fig. 2(b)** shows that stable Ohmic contacts are formed between the channel and S/D in the on-state and that  $I_{\text{DS}}$  increases with increasing gate overdrives ( $V_{\text{GB}} - V_{\text{PI}}$ ). **Fig. 2(c)** shows that  $V_{\text{PI}}$  for the case where input voltages are applied to both of the two gates (i.e., “double-gate” operation) is smaller than that for the two cases where inputs are applied to either one of the gates (“single-gate” operation).  $V_{\text{PI}}$  for the single-gate operations (with input combinations—either [1 0] or [0 1]) are different from each other due to positive strain gradient within the movable structure, i.e., the actuation gap ( $g_0$ ) near the center of the movable structure is slightly smaller (by  $\sim 25 \text{ nm}$ ) than that at the edge. Measured timing diagrams (in **Fig. 2(d)**) shows that a single double-gate relay can perform either two-input AND or OR functions via adjusting the body bias.

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[1] K. Fukuda *et al.*, *Sci. Rep.*, vol. 4, pp. 3947, 2014.

[2] C. D. Dimitrakopoulos *et al.*, *Adv. Mater.*, vol. 14, pp. 99–117, 2002.

[3] J. Jeon *et al.*, *Electron Device Lett.*, vol. 33, pp. 281–283, 2012.

[4] Y. Pan *et al.*, *Trans. Electron Devices*, vol. 63, pp. 832–840, 2016.

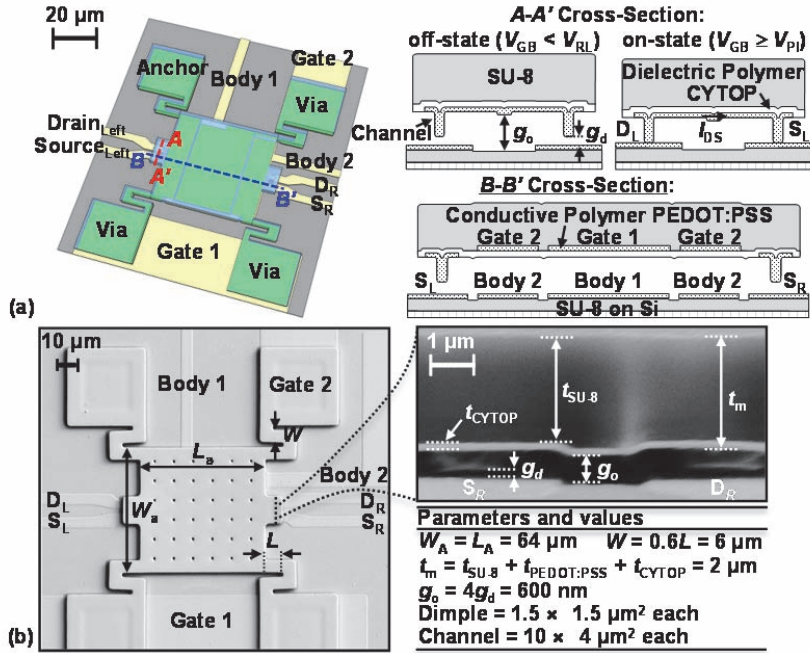


Fig. 1: (a) Isometric schematic and cross-sectional views; (b) SEMs and design parameters.

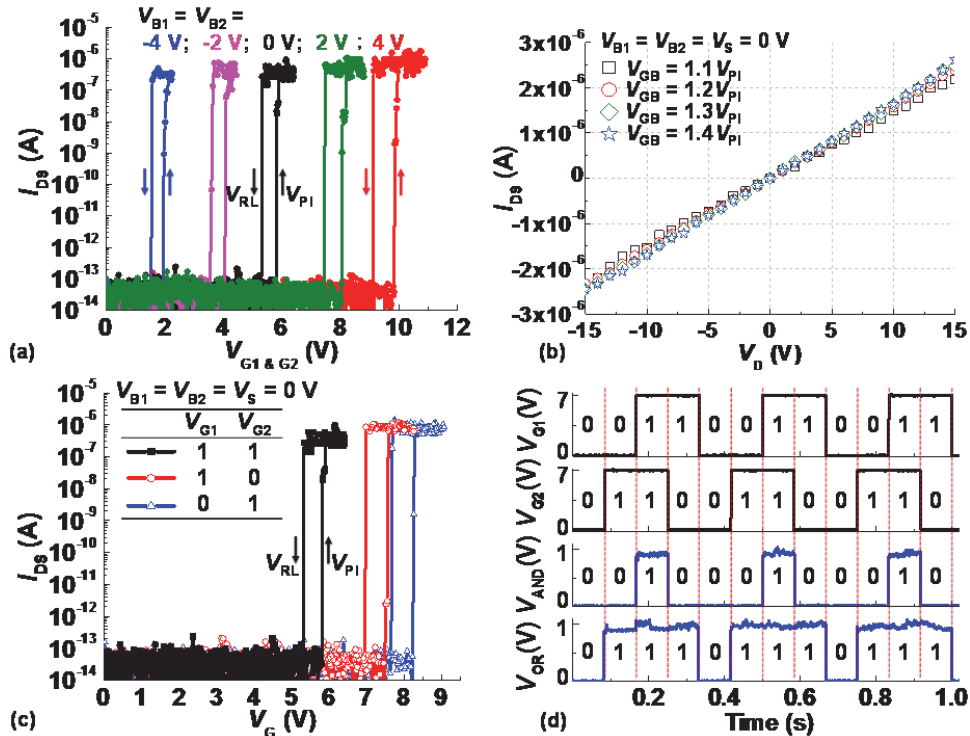


Fig. 2: (a) Measured  $I_{DS}-V_G$  for various body bias voltages.  $V_D = 1.1V_{PI}$ .  $V_S = 0 \text{ V}$ ; (b) Measured  $I_{DS}-V_D$  for different gate overdrive voltages.  $V_G = V_{G1} = V_{G2}$ ; (c) Measured  $I_{DS}-V_G$  for different input voltage combinations. "1"  $\equiv V_G$ .  $V_D = 1.1V_{PI}$ ; (d) Measured timing diagrams for AND and OR gates.  $V_B = 0 \text{ V}$  for AND,  $V_B = -2 \text{ V}$  for OR,  $V_D = 7 \text{ V}$  and  $V_S = 0 \text{ V}$ .