A New Opportunity to Fabricate Multi-Bit Transistor Memories Using Mechanically Exfoliated Multilayer WSe_2 Flakes

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It is still desirable to explore new simple nano/microfabrication approaches that can create low-cost solid-state drives (SSDs) based on field-effect transistor (FET) memories. 2D semiconducting layered transition metal dichalcogenides (TMDCs, *e.g.*, MoS_2 and WSe_2) are anticipated to provide new opportunities in this research area[1,2]. However, most recent efforts have been focused on the direct application of TMDC FET channels into the conventional FET-based memory structure consisting of regular floating gates, tunnel barriers, or charge trapping layers.[3,4] Such memory devices still have quite complicated architectures, and such works have not effectively reduced the complexity and cost of solid-state memory manufacturing. Recently, we found that an exfoliated multilayer MoS_2 flake (Fig. 1a), after a plasma doping process, has a rough (or rippled) top layer (Fig. 1b). When incorporated into a FET structure (Fig. 1c), this rough layer can serve as a charge-trapping layer interfacing with the underlying pristine layers that serve as the FET channel. This device structure can function as a FET memory and enable multi-bit data storage (*i.e.*, year-scale binary or 2-bit data storage; day-scale 3-bit data storage (see Fig. 1d)).[2] This work has preliminarily leveraged the unique layered structure of TMDCs for making ultra-low-cost memory devices.

Here, we further report that a mechanically exfoliated multilayer WSe_2 flake can directly serve as a FET memory channel with no need of plasma doping and enable multi-bit data storage functionality. This finding could further simplify the fabrication steps for producing SSDs.

The newly observed memory states in multilayer WSe_2 are tentatively attributed to the vulnerability of WSe_2 layers to mechanical exfoliation. This means that the mechanical exfoliation of a multilayer WSe_2 flake from a bulk WSe_2 stamp could directly result in a rough (or rippled) top layer on the exfoliated flake, as illustrated in Fig. 2a. Such a rough WSe_2 top layer, similar to the plasma-doped MoS_2 top layer illustrated in Fig. 1b, could serve as a charge-trapping layer for the FET memory and enable multi-bit data storage (Fig. 2b). Fig. 2c shows the retention characteristics of a set of 2-bit (*i.e.*, 4 data levels) memory states measured from a representative WSe_2 FET memory, which are comparable to the memory states obtained from a plasma-doped MoS_2 FET memory (Fig. 1d). To support our hypothesis, we further characterized as-exfoliated WSe_2 and MoS_2 flakes using atomic force microscopy (AFM) (Fig. 3). The AFM results show that as-exfoliated multilayer WSe_2 flakes exhibit a much larger surface roughness in comparison with as-exfoliated multilayer MoS_2 flakes. This result strongly supports our hypothesis on the exfoliation-induced memory states in multilayer WSe_2. Additional work will be performed to understand the physical origin of the vulnerability of WSe_2 layers to mechanical exfoliation and evaluate the reliability/uniformity of multilayer WSe_2 FET memories.

In addition to advance the fabrication technology for producing low-cost memories, this work also provides important scientific insights for creating new nanoelectronic devices through mechanically processing emerging layered materials.

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[2] Chen, Mikai, et al.ACS nano 8.4 (2014): 4023-4032.
[3] Choi, Min Sup, et al. Nature communications 4 (2013): 1624.
[4] Jariwala, Deep, et al. ACS nano 8.2 (2014): 1102-1120.

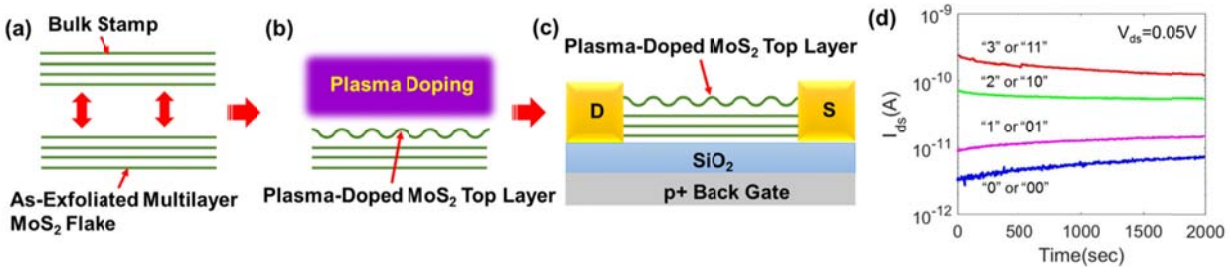

Figure 1: Illustrations of (a) an as-exfoliated multilayer MoS_2 flake with a smooth top layer, (b) a plasma-doped MoS_2 flake with a rough (or rippled) top layer, and (c) a FET memory with the plasma-doped MoS_2 flake as the FET channel. (d) displays the retention characteristics of 2-bit data storage states in a typical FET memory made from a plasma-doped multilayer MoS_2 flake.

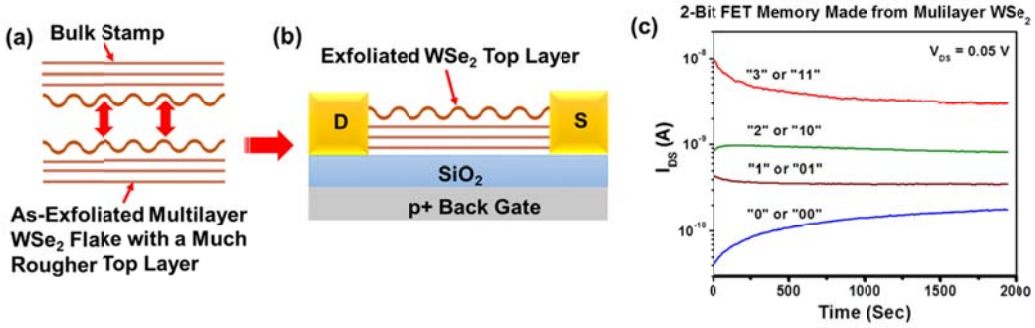

Figure 2**:** Illustrations of (a) an as-exfoliated multilayer WSe_2 flake with a rough (or rippled) top layer, and (b) a FET memory with the exfoliated WSe_2 flake as the FET channel. (c) displays the retention characteristics of 2-bit data storage states in a typical FET memory made from an as-exfoliated multilayer WSe_2 flake.

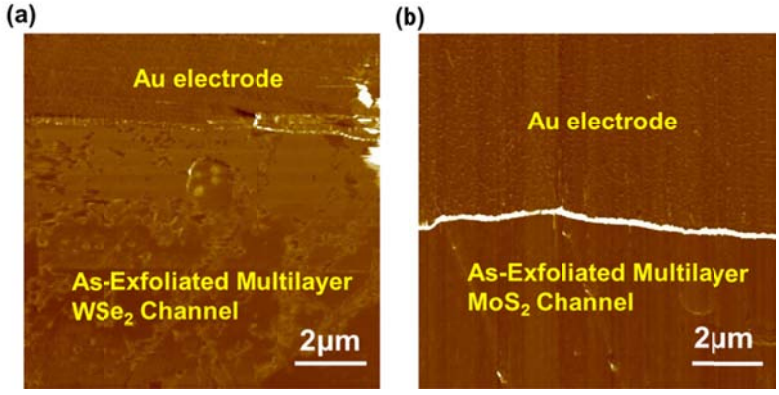

Figure 3: AFM images of the top surfaces of (a) an as-exfoliated multilayer WSe_2 flake and (b) an as-exfoliated multilayer MoS_2 flake. The WSe_2 flake exhibits a much larger top surface roughness (RMS value: 5.6 nm) in comparison with the MoS_2 flake (RMS value: 2.7 nm).