Mask registration and array efficiency for nitride FinFET prototyping

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As the scaling of device technology continues past the 15 nanometer technology node, it is imperative that power devices and high performance RF devices find a common platform. Nitride devices that have high electron gas density and resulting in high mobility, need to be integrated in high performance power devices with CMOS FinFET technology. As such devices are lithographically carved into the 2D electron gas, nano-scale strain changes are induced in local areas in a manner depending on geometry. An understanding of the feature size and its impact based upon electron gas composition has been studied, but a complete picture is not currently portrayed in the literature. Further understanding of how to design and prototype 3D devices in nitrides, including 2D and drift devices, is required to keep the production platforms similar so that complete integration of silicon and nitride devices is accomplished. To this end, we examine the requirements of wide band gap nitride device technology using electron beam lithography. The extreme difficulty in etching, pattern transfer and hard masking an already extremely hard material is discussed and prototyping processes for mask to mask pattern registration is explored. Geometry dependence of the 2D electron gas density is also described in terms of stress relaxation. Further patterning technology of wide band gap materials for applications in integrated MMICs and nanoantennas is explored.

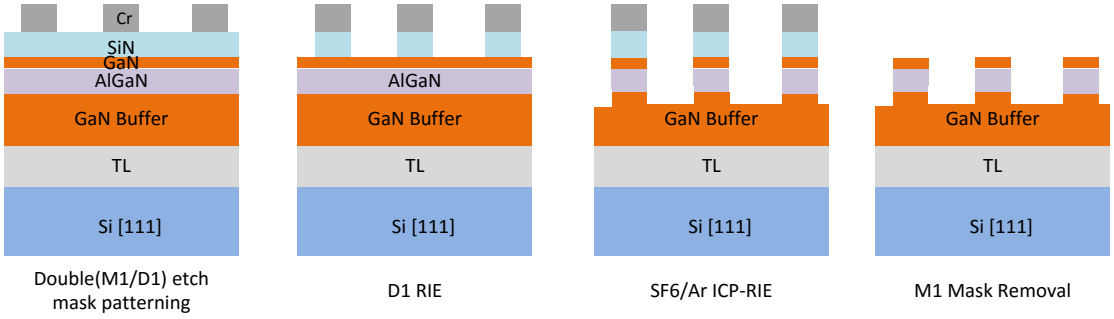

Figure. 1. III-V fin Structure Isolation Process Flow

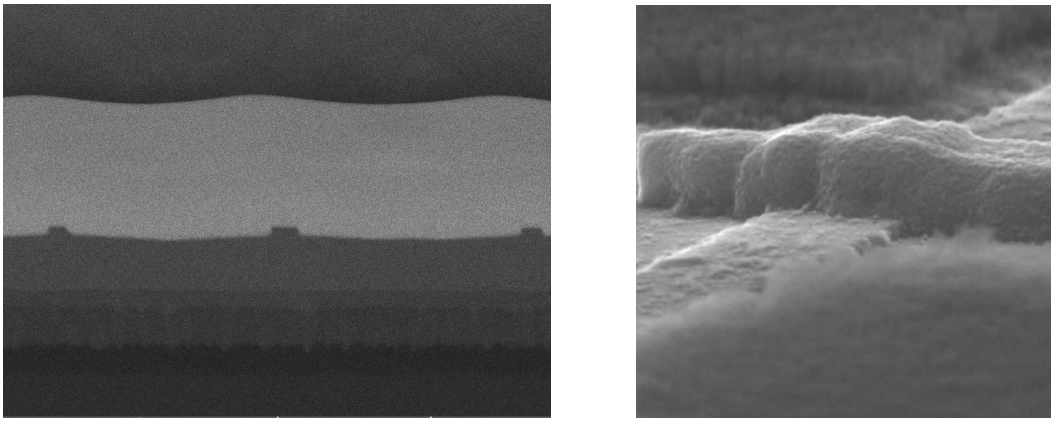

Figure. 2. Fabricated III-V finFET: (a) different channel widths of finFET and (b) nano-scale gate/ALD grown dielectric on the nano-fin (NF) in the finFET.

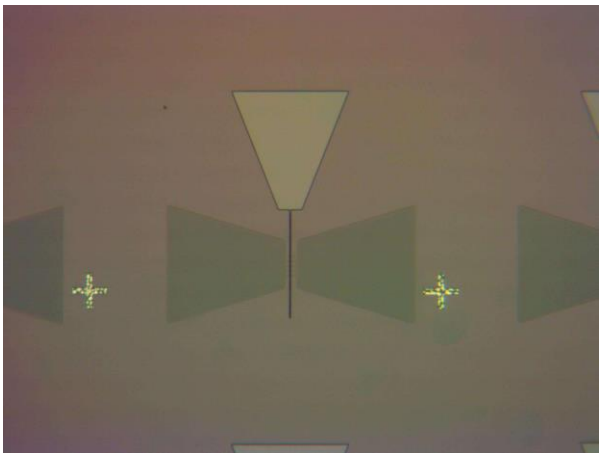

Figure. 3. III-V finFET Fabricated Using Prototyping Processes for Mask to Mask Pattern Registration