III-V NanoWires for Junctionless Transistors Fabricated by Focused Ion Beam (FIB) System

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III-V Junctionless semiconductors devices were fabricated on InGaP and GaAs substrates using Gallium (Ga^+) Focused Ion Beam (FIB) System. Two groups of samples, with N+-InGaP (10 nm)/GaAs-buffer layer (300 nm) and N+-GaAs (10 nm)/GaAs-buffer layer (300 nm), both on semi-insulating GaAs (001) nominal orientation substrates, were studied. The growth was carried out by Chemical Beam Epitaxy (CBE) using triethylgallium and trimethylindium as Ga and In sources, respectively, and thermally cracked hydrides, PH_3 for InGaP and AsH_3 for GaAs, as group V sources. The growth temperature was 550^{o}C and solid silicon was used for doping the epitaxial layers. The morphology of the samples was observed by Atomic Force Microscopy (AFM). X-Ray diffraction (XRD) analysis was used in order to determine the InGaP lattice parameter and mismatch to the GaAs substrate. Hall measurements provided silicon doping levels of 10^{+18} cm^{-3} for both groups of samples, indicating the formation of N+-type layers. These samples were used for MOS Junctionless (JL) Transistors applications, since III-V semiconductors present higher electron mobility values than silicon. Gallium Focused Ion Beam have been used to define the III-V (InGaP or GaAs) nanowires (III-V NWs) (Fig. 1) and also the three terminals of transistors: gate, source and drain. The nanowire, e.g., the electron conduction channel between source and drain, were defined by Pt deposition layers (including the definition of gate, drain and source electrodes) (Fig. 2). The characterization was conducted by the extraction of the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and drain-source current (I_{DS}) versus gate-source voltage (V_{GS}) measurements of Junctionless devices. The results are able to indicate the applicability of InGaP or GaAs nanowires in junctionless transistors fabrication.

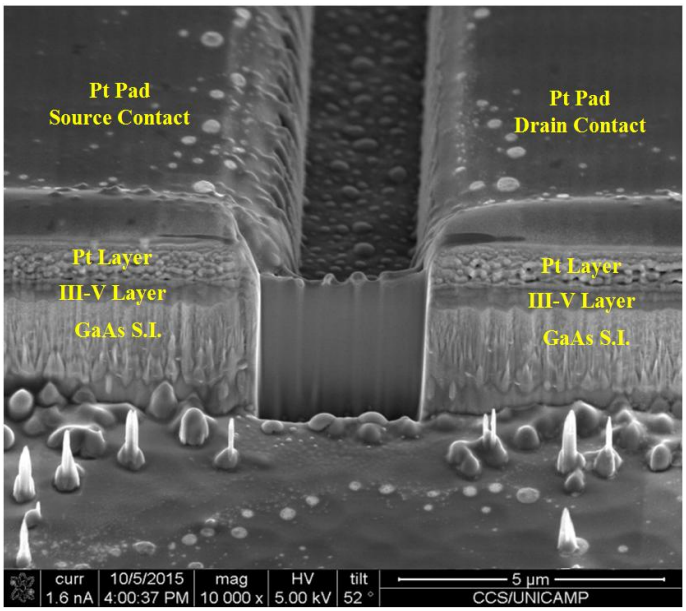

Fig. 1. Definition of III-V (InGaP or GaAs) nanowires (III-V NWs) using FIB.

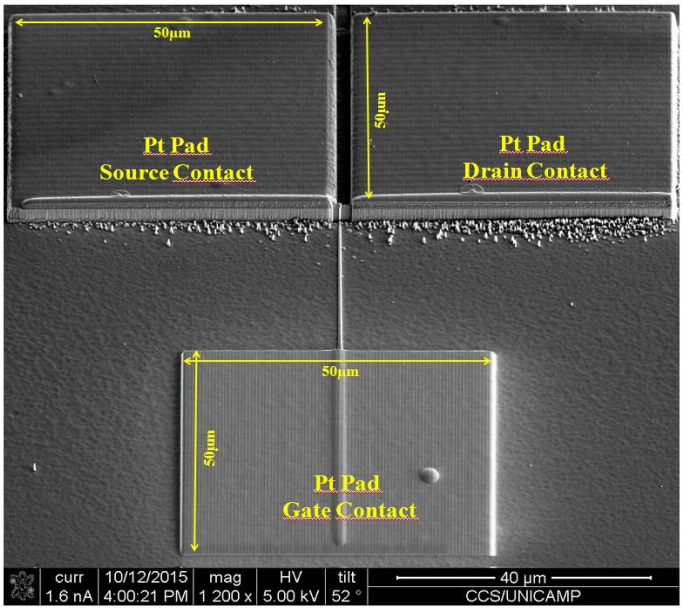

Fig. 2. Definition of gate, drain and source electrodes using FIB.