Fabrication of self-rectifying 3D all-silicon memristor crossbar arrays by stacking fluid supported single-crystalline membranes

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With resistance states representing digital or analog information, high density memristor (or resistive switching devices) crossbar arrays are promising candidates for the next-generation non-volatile memory [1] and brain-inspired computing [2]. However, CMOS compatibility of new materials and 'sneak path' current in a passive array remain challenges for such applications. Here, we report the fabrication and electrical measurements of 3D p-Si/SiO_x/n-Si memristive crossbar arrays that address both issues. The all silicon based materials offers the best CMOS compatibility. The unique device stack enables built-in diodes at each cell which alleviates the sneak path problem.

The device structure is schematically shown in **Fig.1a**. The 70 nm thick bottom electrode is n-type doped single crystalline silicon while the 70 nm thick top electrode is p-type. The switching layer of about 5 nm SiO_2 was grown on the silicon electrode by the hybrid of chemical (Piranha) and oxygen plasma treatment. The electrodes were transferred from silicon device layer of SOI wafers using a fluid supported approach (**Fig.1b-e**), as reported at EIBPN 2014[3]. **Fig.2a** shows the high yield fabrication result of a 64×64 crossbar array. A thin layer of aluminum was deposited on the fanout to reduced wire resistance and contact resistance during measurements. During the electrical measurement, the voltage was applied on contact pads connecting to the top electrode while bottom electrode grounded. After forming, the device could be switched between a high resistance state (HRS) and a rectifying low resistance state (LRS) **(Fig.2b)**. The ON/OFF resistance ratio is about 10^4 while rectification ratio is 10^5, which enables a large passive memristor crossbar array operation.

To demonstrate the feasibility of 3D array operation, we built a 2-layers 8×8 crossbar arrays of self-rectifying all silicon devices by repeating the membrane transfer and patterning process. An HSQ layer was spun-on and annealed for interlayer isolation and planarization. Vias to expose contact pads were patterned and etched for electrical measurement after the arrays were completed. The fabrication process is at room-temperature and thus compatible with back-end-of-line (BEOL). The outer contact pads are connected to the 1st layer crossbar while the inner pads are for the 2nd layer (**Figs.3a, 3b**) We successfully programed the array to store the binaries representing ascii code of "umass" and "amherst" respectively in each layer (**Fig.3c).** The sneak paths within each layer were suppressed by the self-rectifying diode at each cell so that programming and reading of the array were successfully achieved.

The crossbar arrays may also be stacked into 3D without using the HSQ isolation layers. By stacking p- and n-Si alternatively, each electrode is shared by two adjacent layers, further increasing the packing density. The interlay sneak path current is effectively blocked by the built-in diodes along the path (**Fig.4a**). We stacked 6 layers of silicon nanowires, with SiO_2 in between, that made 5-layers of memristor crossbars (**Fig. 4b**). The nanowire electrodes have a cross-section size of 100 nm×70 nm, a pitch of 200 nm. Our simulation (**Fig.4c**) shows that with a self-rectifying ratio of 10^5 for a 64×64 array and there is little difference in ON/OFF ratio when the layer number is larger than 3. The results suggest that stacking more layers into 3D does not introduce more sneak path current in the array operation.

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[3] T. Tuma, A. Pantazi, M.L. Gallo, A. Sebastian & E. Eleftheriou, Nat. Nanotechnol., **11**, 693 (2016)

[4] C. Li & Q. Xia, EIPBN 2014

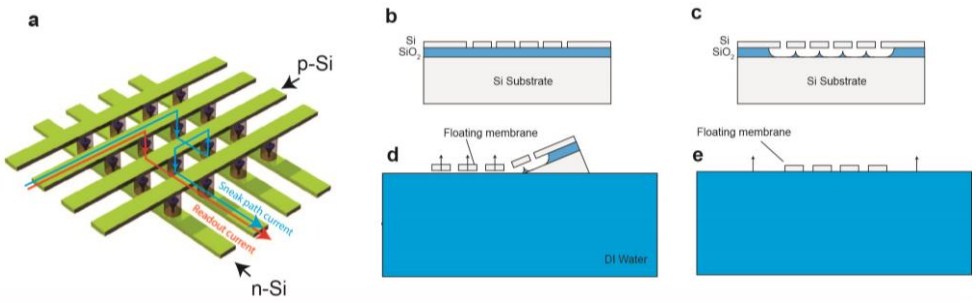

Figure 1: ***(a)*** *Schematic for device structure and sneak path problem. The blue line is one example sneak path that includes one reverse biased cell, which significantly reduces the sneak path current.* ***(b)*** *An SOI wafer is patterned into mesh structure using photolithography and dry etching.* ***(c)*** *HF etching undercuts buried oxide through the patterned holes.* ***(d)*** *The silicon membrane is peeled off from the substrate by capillary force, and floats on the surface of the DI water;* ***(e)*** *The membrane is picked up by another substrate.*

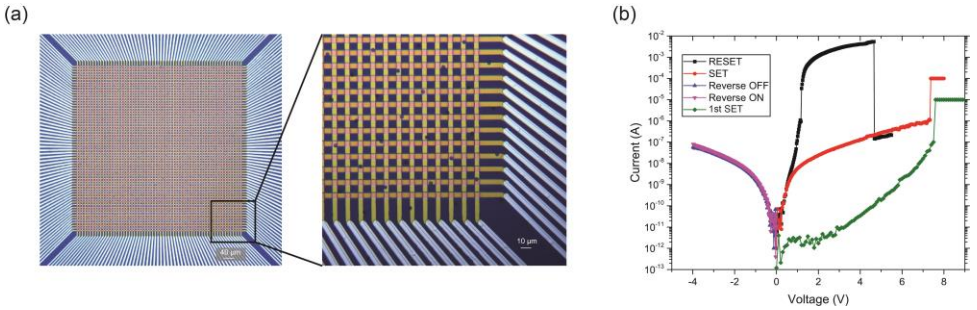

Figure 2: ***(a)*** *Fabrication result for a 64×64 crossbar array. The zoomed image shows the metal aluminum was deposited on the fanout to reduce the wire resistance. The devices in the arrays have a junction size of 5μm×5μm.* ***(b)*** *The typical resistive switching IV curve for a single device, which shows the ON/OFF ratio was more than 10^4 and rectifying ratio almost 10^5 when bias voltage was larger than +1.5 V.*

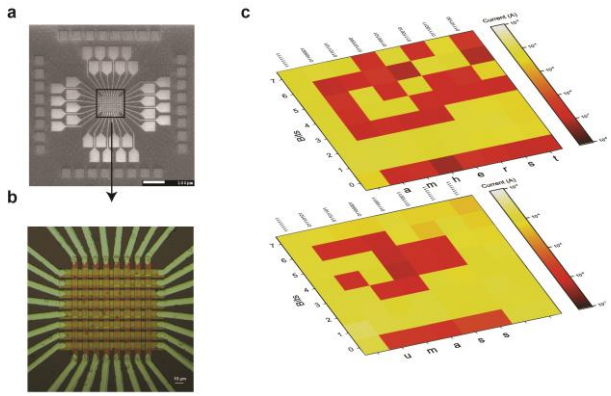

Figure 3: **(a)** *SEM image of the 2-layer stacked 8×8 memristors array. For the 1st layer structure, only the measurement pads can be clearly seen in this image as other parts are buried inside of the interlayer dielectric.* ***(b).*** *Magnified image of the optical image for the crossbar devices. One sees both layer structures due to slight misalignment between layers.* ***(c)*** *The color map of the readout current at +2V for the 2 layers stacked memristors which were programmed into "umass" and "amherst" respectively. All other cells were programmed into LRS to maximize the sneak path current to consider the worst case scenario.*

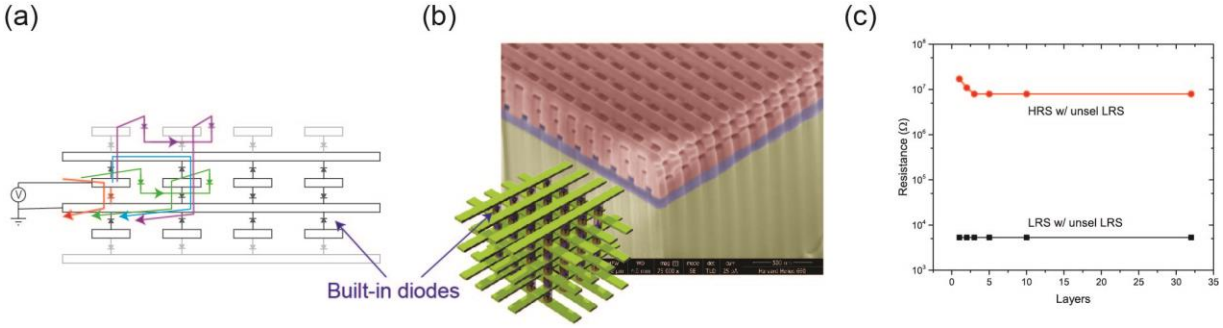

Figure 4: ***(a)*** *Cross sectional schematic for 3D stacking with shared bit/word line between adjacent layers. The blue curve shows one possible interlayer sneak path and the green one the in-layer sneak path. The purple line shows sneak path go through beyond one layer on top of selected layer will inevitably include at least 3 reverse biased device, which limits sneak path current orders of magnitude smaller.* ***(b)*** *The bird-eye view SEM image shows the fabrication results for the 3D stacked silicon crossbar devices with shared bit/word line configuration, and the inset shows the 3D schematic.* ***(c)****, Simulated readout resistance in different states in a 64×64 array with different layer number considering the worst case scenario. The readout result show little difference when the layer number is larger than 3.*