Fabrication of Multi-Bit Memory Devices Based on Layered Semiconductors *via* Interlayer Deformation

Mikai Chen, Yifan Wang, L. Jay Guo, and Xiaogan Liang*
Department of Mechanical Engineering, University of Michigan, Ann Arbor, MI 48109

The cutting-edge technology areas, such as hardware-level artificial intelligence (AI) machines, fly-by-feel control systems for next-generation vehicles, and neuromorphic ICs for advanced learning machines, need novel solid-state memory solutions with a lower cost-per-bit, a better scalability in comparison with the state-of-the-art memory devices, and new logic components with multiple (or analog-tunable) levels of excitation (or data storage) states.[1-2] Several prototype devices have been fabricated and tested to realize multibit (or analog) memory states. For example, Shen *et al.* demonstrated neuromorphic modules based on randomly dispersed carbon nanotubes (CNTs).[3-4] Lu *et al.* fabricated synaptic memory systems based on memristor devices.[5] Additional upscalable nanofabrication methods capable of generating reliable analog memory states in electronic materials are highly desirable.

Here, we report that the nanoimprint-assisted shear exfoliation process can generate interlayer deformation features in exfoliated layered semiconductor (*e.g.*, transition metal dichalcogenides (TMDCs)) structures. Such deformation features can result in charge memory states with long retention times, relatively large extrema spacings, and analog tunability.

Fig. 1a schematically illustrates the shear exfoliation process for producing few-layer TMDC device structures. **Fig. 1b** shows the high-resolution TEM image of the cleaved surface of an as-exfoliated few-layer WSe_2 flake. This cleaved surface exhibits a quasi-periodic Moire pattern, which indicates the existence of exfoliation-induced interlayer deformation features (*e.g.*, interlayer twists or ripplocations) in the few-layer WSe_2 flake. Based on our density functional theory (DFT) simulation results, such interlayer deformation structures are expected to result in charge-trapping states with large binding energies and therefore long charge-retention times. Our FETs made from such exfoliated few-layer WSe_2 flakes exhibit long-lasting, metastable charge memory states with large extrema spacings and analog tunability, as demonstrated in **Fig. 1c**, which strongly supports the expectation from the DFT simulation. We further demonstrated that such multiple charge memory states have a good cycling durability, as demonstrated by the cycling endurance test result in **Fig. 2a**. Through investigating the temperature-dependent retention characteristics of few-layer WSe_2 FETs, we estimated the binding energies of holes and electrons in exfoliated few-layer WSe_2 flakes to be 0.7 and 0.4 eV, respectively. In the presentation, we will further present the neuromorphic signal processing results using our few-layer WSe_2 FETs with exfoliation-induced interlayer deformation structures.

This work advanced the critical nanofabrication and materials processing technologies for leveraging the unique charge-retention and mechanical properties of TMDC layers for new memory-related applications.

1. DiVincenzo, D. P. Toward Control of Large-Scale Quantum Computing. *Science* **2011**, 334, 50-51.
2. Koch, C. Computation and the single neuron. *Nature* **1997**, 385, 207-210.
3. Shen, A. M.; Chen, C.-L.; Kim, K.; Cho, B.; Tudor, A.; Chen, Y. Analog neuromorphic module based on carbon nanotube synapses. *ACS nano* **2013**, 7, 6117-6122.
4. Shen, A. M.; Kim, K.; Tudor, A.; Lee, D.; Chen, Y. Doping Modulated Carbon Nanotube Synapstors for a Spike Neuromorphic Module. *Small* **2015**, 11, 1571-1579.
5. Yang, Y.; Chen, B.; Lu, W. D. Memristive physically evolving networks enabling the emulation of heterosynaptic plasticity. *Advanced Materials* **2015**, 27, 7720-7727.

* Email: xiaoganl@umich.edu

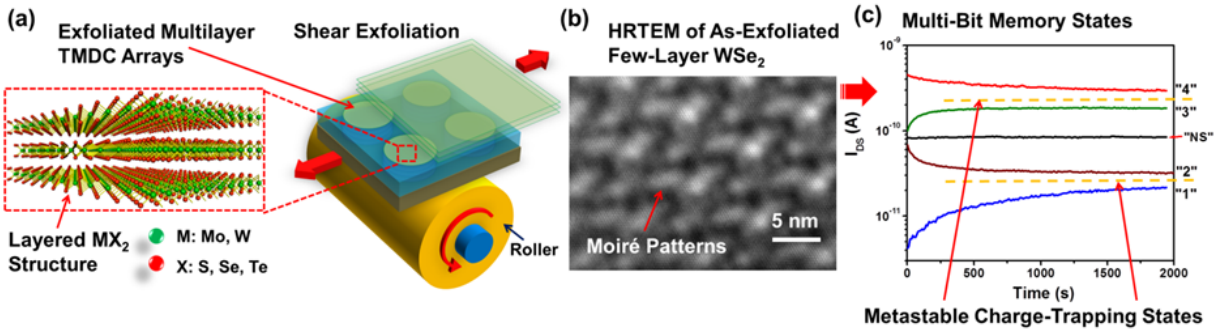

Fig. 1 (a) Schematic illustration of shear exfoliation, (b) High-resolution TEM image of the cleaved surface of a few-layer WSe_2 flake, (c) retention characteristics of a few-layer WSe_2 FET.

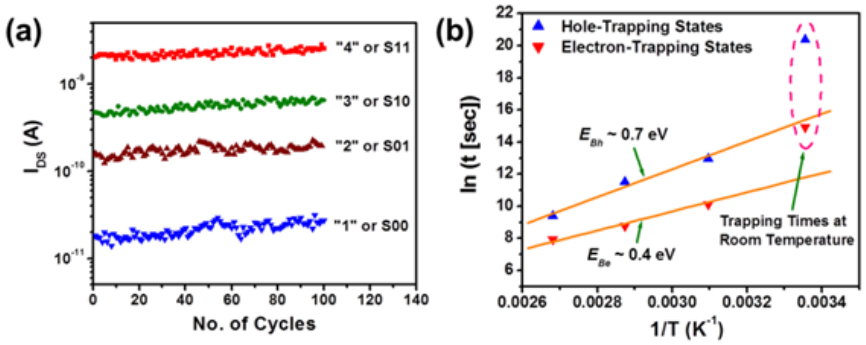

Fig. 2 (a) Cycling endurance test result of a 2-bit WSe_2 FET memory, (b) Trapping times (t) of hole-trapping and electron-trapping states in a few-layer WSe_2 FET, plotted as a function of temperatures, from which the binding energies for holes and electrons are extracted to be 0.7 and 0.4 eV, respectively.

* Email: xiaoganl@umich.edu