High resolution thermal scanning probe lithography for the fabrication of sub-20 nm nanodevices

Yu Kyoung Ryu [a], Colin Rawlings [b], Martin Spieser [b], Heiko Wolf [a], Urs Duerig [a], Sajedeh Manzeli[c], Andras Kis[c], Zahid A. K. Durrani[d], Mervyn Jones[d], Siegfried Karg[a], Vanessa Schaller[a] and Armin W. Knoll [a]

[a] IBM Research − Zurich, Rueschlikon, Switzerland
[b] SwissLitho AG – Zurich, Switzerland
[c]LANES group, Ecole Polytechnique Federale de Lausanne – Lausanne, Switzerland
[d]Imperial College London-London, United Kingdom

e-mail: ryu@zurich.ibm.com

Thermal scanning probe lithography (t-SPL) is a technique that has achieved resolutions of <10 nm, linear patterning speeds of >10 mm/s [1], and less than 5 nm error for overlay accuracy on nanoscale devices buried under the resist stack [2]. A dedicated pattern transfer process has been developed to successfully achieve pattern transfer by reactive ion etching of 18 nm half pitch lines and metal lift-off of sub 20 nm features [3]. We worked to further enhance the resolution by an optimization of the transfer stack. Figure 1a shows an SEM image of an array of Si nanowires (SiNWs) with half pitches of 14 nm and 16 nm. A TEM cross section (Figs. 1b and c) from the 14 nm half pitch patterns demonstrates the potential of t-SPL to fabricate sub-10 nm wide SiNWs. As an additional development, we complemented the tool by integrating a 375 nm laser for mix and match of laser writing and t-SPL patterning in the same resist layer to enable fast processing of bigger low resolution fields such as contact pads.

We demonstrate the capabilities of the tool by creating devices with high resolution features in various substrates. In silicon we fabricated single electron memory devices with sub 25 nm dimensions in a 12 nm thick silicon layer (figs. 2(a), (b)). Leads to the outside were fabricated in the same patterning step by laser writing. On MoS_2 substrates we patterned large arrays of nanoribbons with sub 20 nm dimensions and a length of 100-300 nm to create nanoribbon FET devices (figs 2(c), 2(d)). Using InAs nanowires, we fabricated source and drain contacts with down to 50 nm distance and observed quantized conductance in the channels at 80 K with a 90% injection efficiency (figs 2(e), 2(f)) and a steep switch on-off behavior using top gates.

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References:

[1] P. Paul et al., *Nanotechnology* **23**, 385307 (2012)
[2] C. Rawlings et al., *ACS Nano* **9**, 6188-6195 (2015)
[3] H. Wolf et al., *J. Vac. Sci. Technol. B* **33**, 02B102 (2015)

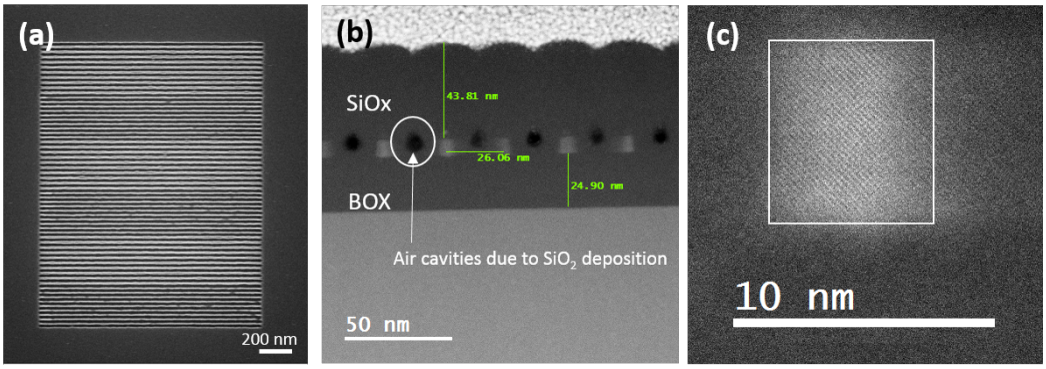

Figure 1: (a) Array of 14 nm and 16 nm half pitch SiNWs after t-SPL lithography and pattern transfer processing. (b) TEM cross section image of an array of sub-10 nm wide SiNWs. (c) TEM cross section showing the crystal lattice of one the SiNWs shown in (b). The white box is a guide to the eye.

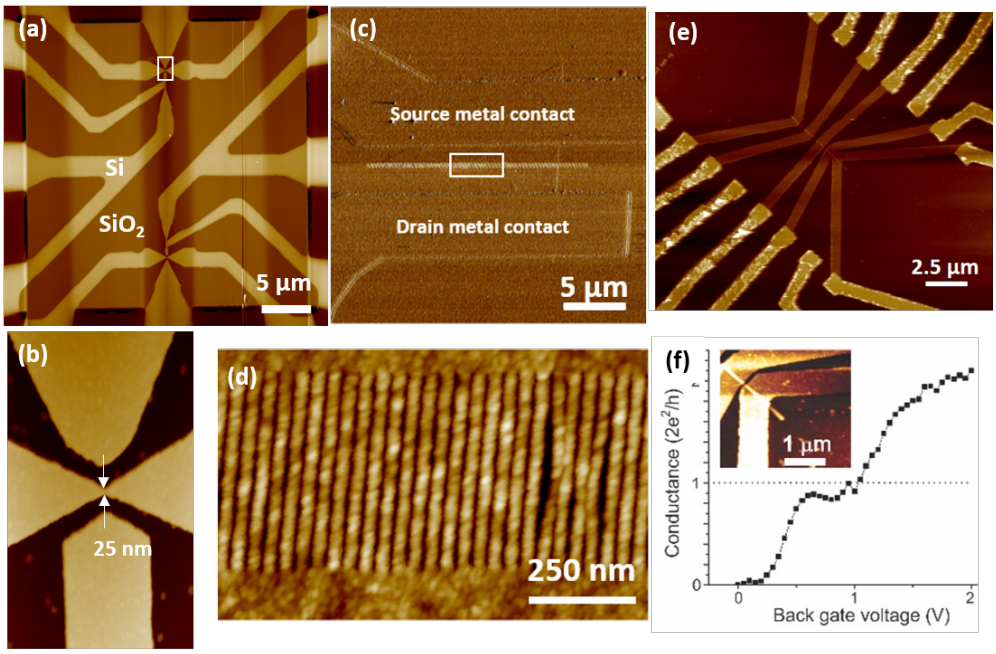

Figure 2: (a) Single electron transistor defined by t-SPL, laser writing and reactive ion etching on an ultrathin silicon on insulator layer. (b) Close-up AFM image of the white rectangle marked in (a). (c) Array of 384 nanoribbons with an half pitch of 18 nm and length of 350 nm patterned on an MoS_2 monolayer with metal contacts. (d) Close-up AFM image of the white rectangle marked in (c). (e) Source to drain contacts of varying distance on a 30 nm diameter InAs NW defined by t-SPL. (f) Ballistic conduction measured at 80 K for the source to drain contact distance of 50 nm. The inset shows the AFM topography of the device.